TMS470R1A64
16/32-Bit RISC Flash Microcontroller

SPNS099B–NOVEMBER 2004–REVISED AUGUST 2006

FEATURES

- High-Performance Static CMOS Technology
- TMS470R1x 16/32-Bit RISC Core (ARM7TDMI™)
  - 24-MHz System Clock (48-MHz Pipeline Mode)
  - Independent 16/32-Bit Instruction Set
  - Open Architecture With Third-Party Support
  - Built-In Debug Module
  - Big-Endian Format Utilized
- Integrated Memory
  - 64K-Byte Program Flash
    - One Bank With Five Contiguous Sectors
    - Internal State Machine for Programming and Erase
  - 8K-Byte Static RAM (SRAM)
- Operating Features
  - Core Supply Voltage (V_{CC}): 1.71 V–2.06 V
  - I/O Supply Voltage (V_{CCIO}): 3.0 V–3.6 V
  - Low-Power Modes: STANDBY and HALT
  - Extended Industrial Temperature Range
- 470+ System Module
  - 32-Bit Address Space Decoding
  - Bus Supervision for Memory and Peripherals
  - Analog Watchdog (AWD) Timer
  - Real-Time Interrupt (RTI)
  - System Integrity and Failure Detection
- Zero-Pin Phase-Locked Loop (ZPLL)-Based Clock Module With Prescaler
  - Multiply-by-4 or -8 Internal ZPLL Option
  - ZPLL Bypass Mode
- Six Communication Interfaces:
  - Two Serial Peripheral Interfaces (SPIs)
    - 255 Programmable Baud Rates
  - Two Serial Communication Interfaces (SCIs)
    - 2^{24} Selectable Baud Rates
    - Asynchronous/Isosynchronous Modes
  - Standard CAN Controller (SCC)
  - 16-Mailbox Capacity
  - Fully Compliant With CAN Protocol, Version 2.0B
  - Class II Serial Interface (C2SIa)
    - Two Selectable Data Rates
    - Normal Mode 10.4 Kbps and 4X Mode 41.6 Kbps
- High-End Timer (HET)
  - 13 Programmable I/O Channels:
    - 12 High-Resolution Pins
    - 1 Standard-Resolution Pin
  - High-Resolution Share Feature (XOR)
  - HET RAM (64-Instruction Capacity)
- 10-Bit Multi-Buffered ADC (MibADC) 8-Channel
  - 64-Word FIFO Buffer
  - Single- or Continuous-Conversion Modes
  - 1.55 μs Minimum Sample and Conversion Time
  - Calibration Mode and Self-Test Features
- 6 External Interrupts
- Flexible Interrupt Handling
- 5 Dedicated General-Purpose I/O (GIO) Pins, 1 Input-Only GIO Pin, and 34 Additional Peripheral I/Os
- External Clock Prescale (ECP) Module
  - Programmable Low-Frequency External Clock (CLK)
- On-Chip Scan-Base Emulation Logic, IEEE Standard 1149.1 (1) (JTAG) Test-Access Port
- 80-Pin Plastic Low-Profile Quad Flatpack (PN Suffix)

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(1) The test-access port is compatible with the IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture specification. Boundary scan is not supported on this device.

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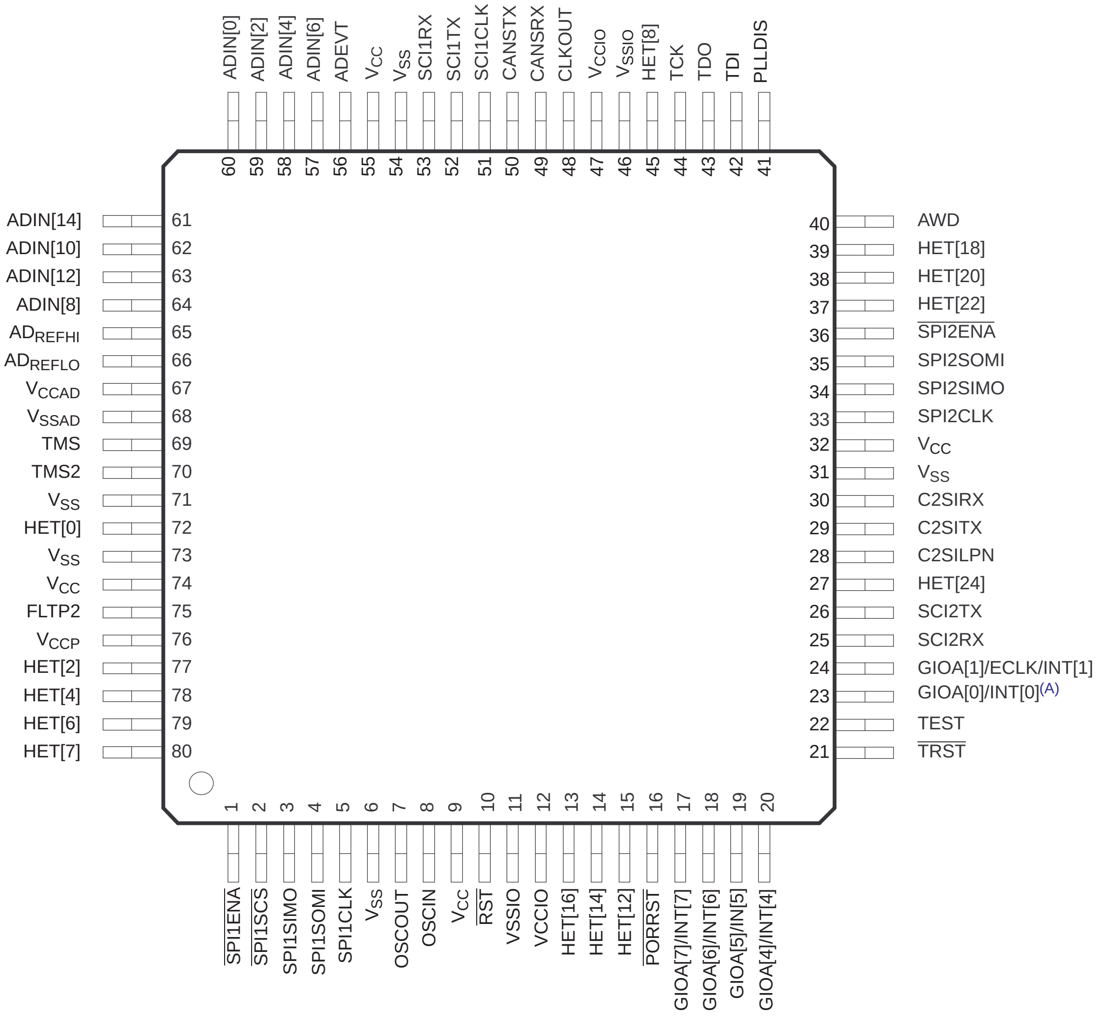
TMS470R1A64 80-PIN PN PACKAGE (TOP VIEW)



A. GIOA[0]/INT0 (pin 23) is an input-only GIO pin.

DESCRIPTION

The TMS470R1A64 (2) device is a member of the Texas Instruments TMS470R1x family of general-purpose 16/32-bit reduced instruction set computer (RISC) microcontrollers. The A64 microcontroller offers high performance utilizing the high-speed ARM7TDMI 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining high code efficiency. The ARM7TDMI 16/32-bit RISC CPU views memory as a linear collection of bytes numbered upwards from 0. The TMS470R1A64 utilizes the big-endian format, where the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The A64 RISC core architecture offers solutions to these performance and cost demands while maintaining low power consumption.

The A64 device contains the following:

- ARM7TDMI 16/32-Bit RISC CPU
- TMS470R1x system module (SYS) with 470+ enhancements
- 64K-byte flash
- 8K-byte SRAM

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(2) Throughout the remainder of this document, the TMS470R1A64 device will be referred to as either the full device name, TMS470R1A64, or as A64.

- Zero-pin phase-locked loop (ZPLL) clock module
- Analog watchdog (AWD) timer
- Real-time interrupt (RTI) module
- Two serial peripheral interface (SPI) modules
- Two serial communication interface (SCI) modules
- Standard CAN controller (SCC)
- Class II serial interface (C2SIa)
- 10-bit multi-buffered analog-to-digital converter (MibADC), 8-input channels
- High-end timer (HET) controlling 13 I/Os
- External Clock Prescale (ECP)
- Up to 39 I/O pins and 1 input-only pin

The functions performed by the 470+ system module (SYS) include:

- Address decoding
- Memory protection
- Memory and peripherals bus supervision
- Reset and abort exception management
- Prioritization for all internal interrupt sources
- Device clock control
- Parallel signature analysis (PSA)

This data sheet includes device-specific information such as memory and peripheral select assignment, interrupt priority, and a device memory map. For a more detailed functional description of the SYS module, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

The A64 memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes.

The flash memory on the A64 device is a nonvolatile, electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The flash operates with a system clock frequency of up to 24 MHz. In pipeline mode, the flash operates with a system clock frequency of up to 48 MHz. For more detailed information on the flash, see the *F05 flash* section of this data sheet and the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

The A64 device has six communication interfaces: two SPIs, two SCIs, an SCC, and a C2SIa. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The SCI is a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals using the standard non-return-to-zero (NRZ) format. The SCC uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The SCC is ideal for applications operating in noisy and harsh environments (e.g., industrial fields) that require reliable serial communication or multiplexed wiring. The C2SIa allows the A64 to transmit and receive messages on a class II network following an SAE J1850 (3) standard.

For more detailed functional information on the SPI, SCI, and SCC peripherals, see the specific TMS470R1x peripheral reference guides (literature numbers SPNU195, SPNU196, and SPNU197, respectively). For more detailed functional information on the C2SIa peripheral, see the *TMS470R1x Class II Serial Interface A (C2SIa) Reference Guide* (literature number SPNU218).

The HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. For more detailed functional information on the HET, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

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(3) SAE Standard J1850 Class B Data Communication Network Interface.

The A64 HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high-resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET. For more detailed information on the HET XOR-share feature, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The A64 device has a 10-bit-resolution sample-and-hold MibADC. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. There are three separate groupings, two of which are triggerable by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode. For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

The zero-pin phase-locked loop (ZPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1–8). The function of the ZPLL is to multiply the external frequency reference to a higher frequency for internal use. The ZPLL provides ACLK to the system (SYS) module. The SYS module subsequently provides the system clock (SYSCLK), real-time interrupt clock (RTICLK), CPU clock (MCLK), and peripheral interface clock (ICLK) to all other A64 device modules. For more detailed functional information on the ZPLL, see the *TMS470R1x Zero-Pin Phase-Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212).

NOTE:

ACLK should not be confused with the MibADC internal clock, ADCLK. ACLK is the continuous system clock from an external resonator/crystal reference.

The A64 device also has an external clock prescaler (ECP) module that, when enabled, outputs a continuous external clock (ECLK) on a specified GIO pin. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (ICLK) frequency. For more detailed functional information on the ECP, see the *TMS470R1x External Clock Prescaler (ECP) Reference Guide* (literature number SPNU202).

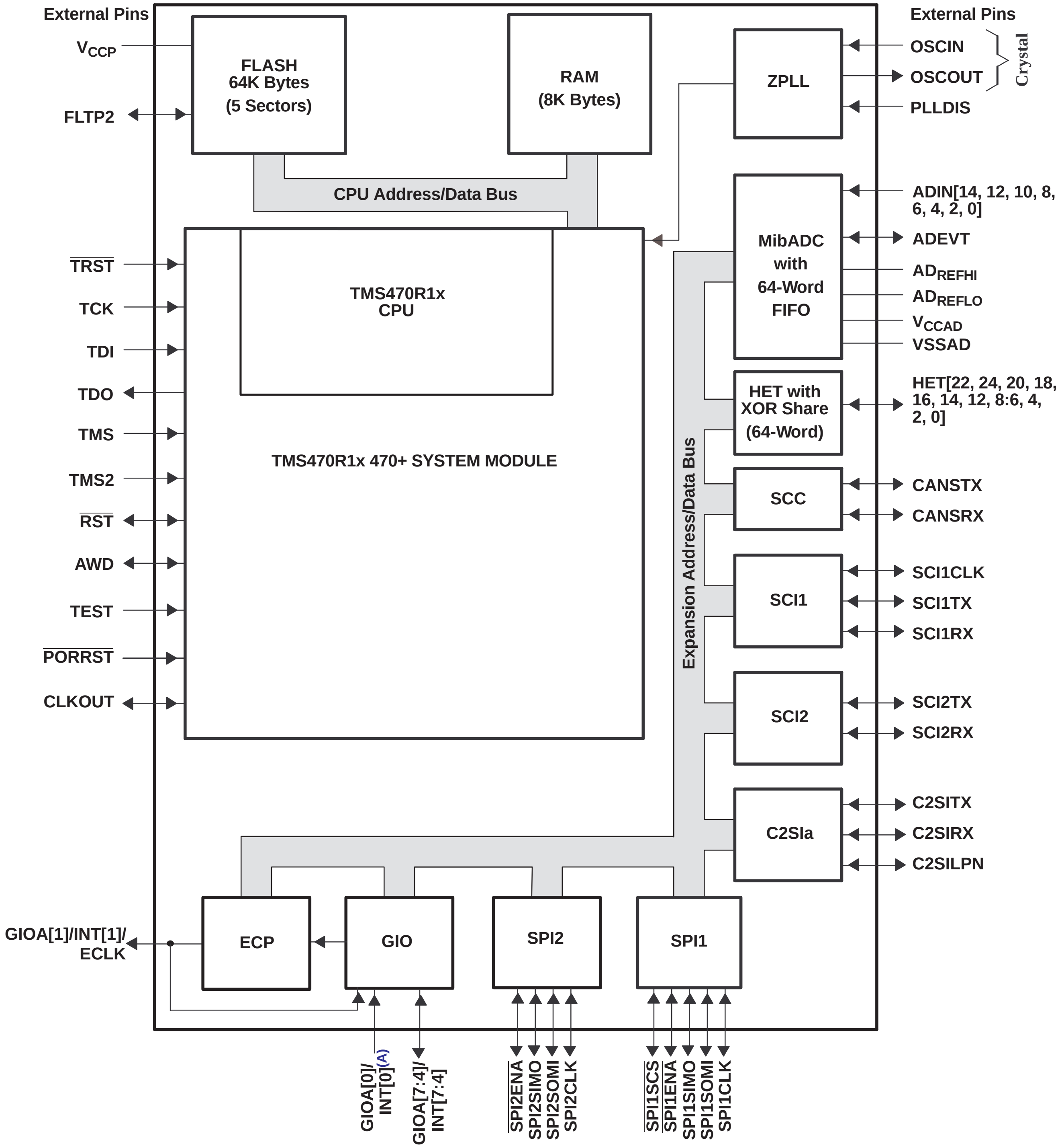
Device Characteristics

The TMS470R1A64 device is a derivative of the F05 system emulation device SE470R1VB8AD. Table 1 identifies all the characteristics of the TMS470R1A64 device except the SYSTEM and CPU, which are generic.

Table 1. Device Characteristics

CHARACTERISTICS	DEVICE DESCRIPTION	COMMENTS
MEMORY		
For the number of memory selects on this device, see the "Memory Selection Assignment" table (Table 3).		
INTERNAL MEMORY	64K-Byte flash 8K-Byte SRAM	Flash is pipeline-capable. The A64 RAM is implemented in one 8K-byte array selected by two memory-select signals (see the "Memory Selection Assignment" table, Table 3).
PERIPHERALS		
For the device-specific interrupt priority configurations, see the "Interrupt Priority" table (Table 6). For the 1K-byte peripheral address ranges and their peripheral selects, see the "A64 Peripherals, System Module, and Flash Base Addresses" table (Table 5).		
CLOCK	ZPLL	Zero-pin PLL has no external loop filter pins.
GENERAL-PURPOSE I/Os	5 I/O 1 Input only	Port A has 6 external pins—GIOA[2]/INT2 and GIOA[3]/INT3 are not available.
ECP	YES	
C2SIa	1	
SCI	1 (3-pin) 1 (2-pin)	SCI2 has no external clock pin, only transmit/receive pins (SCI2TX and SCI2RX)
CAN (HECC and/or SCC)	1 SCC	Standard CAN controller
SPI (5-pin, 4-pin or 3-pin)	1 (5-pin) 1 (4-pin)	SPI2 has no chip select pin.
HET with XOR Share	13 I/O	The A64 device has both the logic and registers for a full 32-I/O HET implemented, even though not all 32 pins are available externally. The high-resolution (HR) SHARE feature allows even-numbered HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET RAM	64-Instruction Capacity	
MibADC	10-bit, 8-channel 64-word FIFO	8-channel MibADC. Both the logic and registers for a full 16-channel MibADC are present.
CORE VOLTAGE	1.71–2.06 V	
I/O VOLTAGE	3.0–3.6 V	
PINS	80	
PACKAGE	PN	

Functional Block Diagram



A. GIOA[0]/INT[0] is an input-only GIO pin.

Table 2. Terminal Functions

TERMINAL		TYPE (1)(2)	INTERNAL PULLUP/ PULLDOWN (3)	DESCRIPTION
NAME	PIN NUMBER			
HIGH-END TIMER (HET)				
HET[0]	72	3.3-V I/O	IPD (20 µA)	The A64 device has both the logic and registers for a full 32-I/O HET implemented, even though not all 32 pins are available externally Timer input capture or output compare. The HET[31:0] applicable pins can be programmed as general-purpose input/output (GIO) pins. HET pins [22, 20, 18, 16, 14, 12, 8, 7, 6, 4, 2, and 0] are high-resolution pins for A64. HET[24] is a standard-resolution pin. The high-resolution (HR) SHARE feature allows even-numbered HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd-numbered pin is available externally. If an odd-numbered pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer Reference Guide* (literature number SPNU199).
HET[2]	77			
HET[4]	78			
HET[6]	79			
HET[7]	80			
HET[8]	45			
HET[12]	15			
HET[14]	14			
HET[16]	13			
HET[18]	39			
HET[20]	38			
HET[22]	37			
HET[24]	27			
STANDARD CAN CONTROLLER (SCC)				
CANSRX	49	3.3-V I/O		SCC receive pin or GIO pin
CANSTX	50	3.3-V I/O	IPU (20 µA)	SCC transmit pin or GIO pin
CLASS II SERIAL INTERFACE (C2SIA)				
C2SILPN	28	3.3-V I/O	IPD (20 µA)	C2SIa module loopback enable pin or GIO pin
C2SIRX	30	3.3-V I/O		C2SIa module receive data input pin or GIO pin
C2SITX	29	3.3-V I/O	IPD (20 µA)	C2SIa module transmit data output pin or GIO pin
GENERAL-PURPOSE I/O (GIO)				
GIOA[0]/INT[0]	23	3.3-V I	IPD (20 µA)	General-purpose input/output pins. GIOA[0]/INT[0] is an input-only pin. GIOA[7:0]/INT[7:0] are interrupt-capable pins. The GIOA[1]/INT[1]/ECLK pin is multiplexed with the external clock-out function of the external clock prescale (ECP) module. GIOA[2]/INT[2] and GIOA[3]/INT[3]] pins are not applicable on the A64 device.
GIOA[1]/INT[1] /ECLK	24	3.3-V I/O		
GIOA[4]/INT[4]	20			
GIOA[5]/INT[5]	19			
GIOA[6]/INT[6]	18			
GIOA[7]/INT[7]	17			
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MibADC)				
ADEVT	56	3.3-V I/O	IPD (20 µA)	MibADC event input. ADEVT can be programmed as a GIO pin.
ADIN[0]	60	3.3-V I		MibADC analog input pins The A64 device has only 8 input channels but all S/W registers are capable. ADIN[15,13, 11, 9, 7, 5, 3, and 1] pins are not applicable to the A64 device.
ADIN[2]	59			
ADIN[4]	58			
ADIN[6]	57			
ADIN[8]	64			
ADIN[10]	62			
ADIN[12]	63			
ADIN[14]	61			
AD_{REFHI}	65	3.3-V REF I		MibADC module high-voltage reference input
AD_{REFLO}	66	GND REF I		MibADC module low-voltage reference input

(1) I = input, O = output, PWR = power, GND = ground, REF = reference voltage, NC = no connect
(2) All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
(3) IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

Table 2. Terminal Functions (continued)

TERMINAL		TYPE(1)(2)	INTERNAL PULLUP/ PULLDOWN(3)	DESCRIPTION
NAME	PIN NUMBER			
V_{CCAD}	67	3.3-V PWR		MibADC analog supply voltage
V_{SSAD}	68	GND		MibADC analog ground reference
SERIAL PERIPHERAL INTERFACE 1 (SPI1)				
SPI1CLK	5	3.3-V I/O	IPD (20 µA)	SPI1 clock. SPI1CLK can be programmed as a GIO pin.
$\overline{\text{SPI1ENA}}$	1			SPI1 chip enable. SPI1ENA can be programmed as a GIO pin.
SPI1SCS	2			SPI1 slave chip select. SPI1SCS can be programmed as a GIO pin.
SPI1SIMO	3			SPI1 data stream. Slave in/master out. SPI1SIMO can be programmed as a GIO pin.
SPI1SOMI	4			SPI1 data stream. Slave out/master in. SPI1SOMI can be programmed as a GIO pin.
SERIAL PERIPHERAL INTERFACE 2 (SPI2)				
SPI2CLK	33	3.3-V I/O	IPD (20 µA)	SPI2 clock. SPI2CLK can be programmed as a GIO pin.
$\overline{\text{SPI2ENA}}$	36			SPI2 chip enable. SPI2ENA can be programmed as a GIO pin.
SPI2SIMO	34			SPI2 data stream. Slave in/master out. SPI2SIMO can be programmed as a GIO pin.
SPI2SOMI	35			SPI2 data stream. Slave out/master in. SPI2SOMI can be programmed as a GIO pin.
ZERO-PIN PHASE-LOCKED LOOP (ZPLL)				
OSCIN	8	1.8-V I		Crystal connection pin or external clock input
OSCOUT	7	1.8-V O		External crystal connection pin
PLLDIS	41	3.3-V I	IPD (20 µA)	Enable/disable the ZPLL. The ZPLL can be bypassed and the oscillator becomes the system clock. If not in bypass mode, TI recommends that PLLDIS be connected to ground or pulled down to ground by an external resistor.
SERIAL COMMUNICATIONS INTERFACE 1 (SCI1)				
SCI1CLK	51	3.3-V I/O	IPD (20 µA)	SCI1 clock. SCI1CLK can be programmed as a GIO pin.
SCI1RX	53	3.3-V I/O	IPU (20 µA)	SCI1 data receive. SCI1RX can be programmed as a GIO pin.
SCI1TX	52	3.3-V I/O	IPU (20 µA)	SCI1 data transmit. SCI1TX can be programmed as a GIO pin.
SERIAL COMMUNICATIONS INTERFACE 2 (SCI2)				
SCI2RX	25	3.3-V I/O	IPU (20 µA)	SCI2 data receive. SCI2RX can be programmed as a GIO pin.
SCI2TX	26	3.3-V I/O	IPU (20 µA)	SCI2 data transmit. SCI2TX can be programmed as a GIO pin.
SYSTEM MODULE (SYS)				
CLKOUT	48	3.3-V I/O	IPD (20 µA)	Bidirectional pin. CLKOUT can be programmed as a GIO pin or the output of SYSCLK, ICLK, or MCLK.
$\overline{\text{PORRST}}$	16	3.3-V I	IPD (20 µA)	Input master chip power-up reset. External V_{CC} monitor circuitry must assert a power-on reset.
$\overline{\text{RST}}$	10	3.3-V I/O	IPU (20 µA)	Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On $\overline{\text{RST}}$, the output buffer is implemented as an open drain (drives low only. To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to $\overline{\text{RST}}$.
WATCHDOG/REAL-TIME INTERRUPT (WD/RTI)				
AWD	40	3.3-V I/O	IPD (20 µA)	Analog watchdog reset. The AWD pin provides a system reset if the WD KEY is not written in time by the system, providing an external RC network circuit is connected. If the user is not using AWD, TI recommends that AWD be connected to ground or pulled down to ground by an external resistor. For more details on the external RC network circuit, see the *TMS470R1x System Module Reference Guide*(literature number SPNU189) and the application note *Analog Watchdog Resistor, Capacitor and Discharge Interval Selection Constraints* (literature number SPNA005).

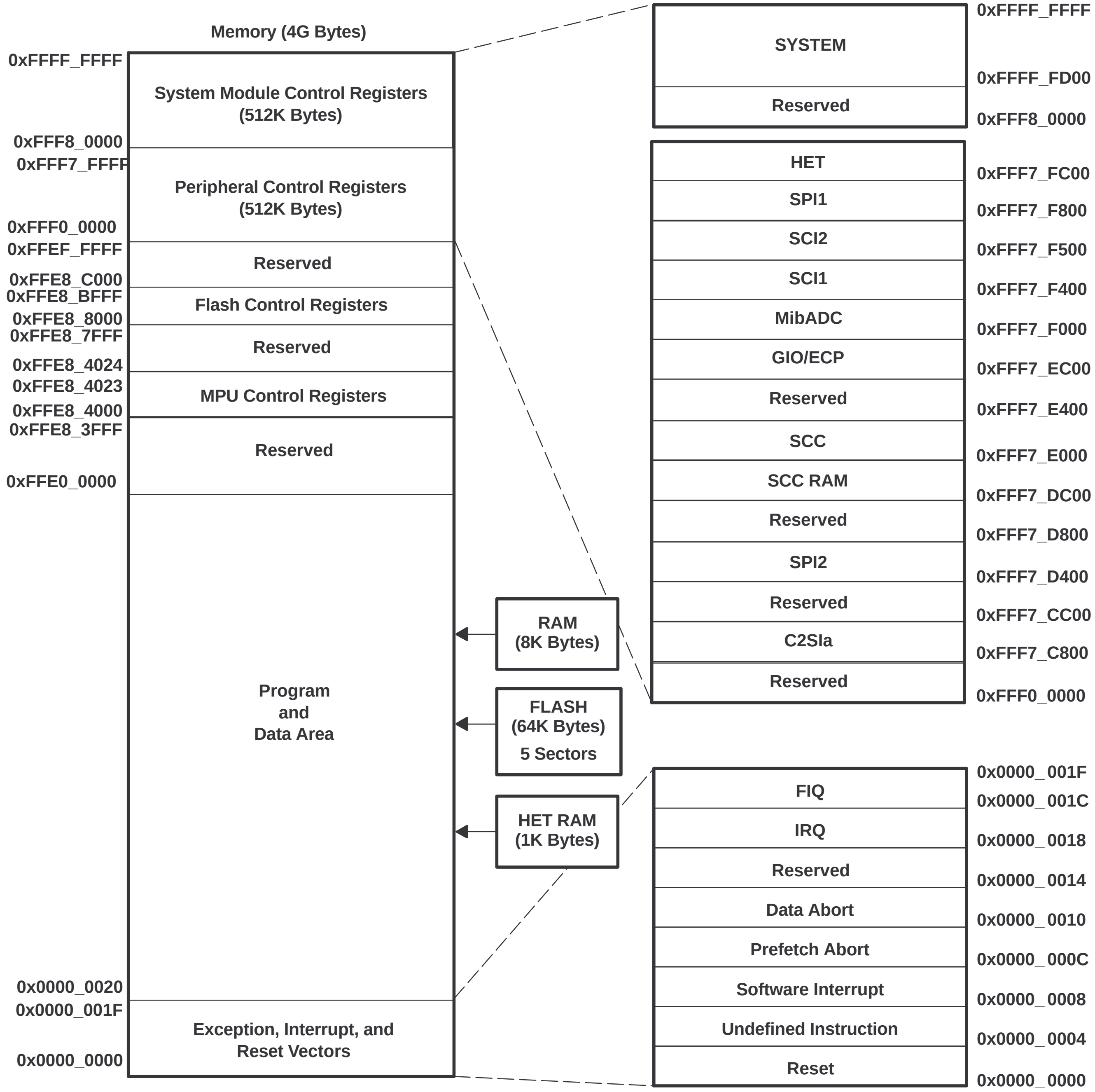
Table 2. Terminal Functions (continued)

TERMINAL		TYPE[1][2]	INTERNAL PULLUP/ PULLDOWN[3]	DESCRIPTION
NAME	PIN NUMBER			
TEST/DEBUG (T/D)				
TCK	44	3.3-V I	IPD (20 µA)	Test clock. TCK controls the test hardware (JTAG)
TDI	42	3.3-V I	IPU (20 µA)	Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG).
TDO	43	3.3-V O	IPD (20 µA)	Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG).
TEST	22	3.3-V I	IPD (20 µA)	Test enable. Reserved for internal use only. TI recommends that TEST be connected to ground or pulled down to ground by an external resistor.
TMS	69	3.3-V I	IPU (20 µA)	Serial input for controlling the state of the CPU test access port (TAP) controller (JTAG)
TMS2	70	3.3-V I	IPU (20 µA)	Serial input for controlling the second TAP. TI recommends that TMS2 be connected to VCCIO or pulled up to VCCIO by an external resistor.
$\overline{\text{TRST}}$	21	3.3-V I	IPD (20 µA)	Test hardware reset to TAP1 and TAP2. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic. TI recommends that $\overline{\text{TRST}}$ be pulled down to ground by an external resistor.
FLASH				
FLTP2	75	NC		Flash test pad 2. For proper operation,FLTP2 must not be connected (no connect [NC]).
V_{CCP}	76	3.3-V PWR		Flash external pump voltage (3.3 V)
SUPPLY VOLTAGE CORE (1.8 V)				
V_{CC}	9	1.8-V PWR		Core logic supply voltage
	32			
	55			
	74			
SUPPLY VOLTAGE DIGITAL I/O (3.3 V)				
V_{CCIO}	12	3.3-V PWR		Digital I/O supply voltage
	47			
SUPPLY GROUND CORE				
V_{SS}	6	GND		Core supply ground reference
	31			
	54			
	71			
	73			
SUPPLY GROUND DIGITAL I/O				
V_{SSIO}	11	GND		Digital I/O supply ground reference
	46			

A64 Device-Specific Information

Memory

Figure 1 shows the memory map of the A64 device.



A. Memory addresses are configurable by the system (SYS) module within the range of 0x0000_0000 to 0xFFE0_0000.

B. The CPU registers are not part of the memory map.

Figure 1. Memory Map

Memory Selects

Memory selects allow the user to address memory arrays (i.e., flash, RAM, and HET RAM) at user-defined addresses. Each memory select has its own set (low and high) of memory base address registers (MFBAHRx and MFBALRx) that, together, define the array's starting (base) address, block size, and protection.

The base address of each memory select is configurable to any memory address boundary that is a multiple of the decoded block size. The decoded block size for the flash is 0x00100000. For more information on how to control and configure these memory select registers, see the bus structure and memory sections of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

For the memory selection assignments and the memory selected, see Table 3.

Table 3. Memory Selection Assignment

MEMORY SELECT	MEMORY SELECTED (ALL INTERNAL)	MEMORY SIZE	MPU	MEMORY BASE ADDRESS REGISTER	STATIC MEM CTL REGISTER
0 (fine)	FLASH	64K	NO	MFBAHR0 and MFBALR0	
1 (fine)	FLASH		NO	MFBAHR1 and MFBALR1	
2 (fine)	RAM	8K(1)	YES	MFBAHR2 and MFBALR2	
3 (fine)	RAM		YES	MFBAHR3 and MFBALR3	
4 (fine)	HET RAM	1K		MFBAHR4 and MFBALR4	SMCR1

(1) The starting addresses for both RAM memory-select signals **cannot** be offset from each other by a multiple of the user-defined block size in the memory-base address register.

RAM

The A64 device contains 8K bytes of internal static RAM configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. This A64 RAM is implemented in one 8K array selected by two memory-select signals. This A64 configuration imposes an additional constraint on the memory map for RAM; the starting addresses for both RAM memory selects cannot be offset from each other by the multiples of the size of the physical RAM (i.e., 8K for the A64 device). The A64 RAM is addressed through memory selects 2 and 3.

The RAM can be protected by the memory protection unit (MPU) portion of the SYS module, allowing the user finer blocks of memory protection than is allowed by the memory selects. The MPU is ideal for protecting an operating system while allowing access to the current task. For more detailed information on the MPU portion of the SYS module and memory protection, see the memory section of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

F05 flash

The F05 flash memory is a nonvolatile electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The F05 flash has an external state machine for programming and erase functions. See the *flash read* and *flash program and erase* sections below.

NOTE:

Flash must be mapped to a boundary of zero or a multiple of 0x00100000. RAM cannot be mapped into the same 0x00100000 space.

flash protection keys

The A64 devices provide flash protection keys. These four 32-bit protection keys prevent program/erase/compaction operations from occurring until after the four protection keys have been matched by the CPU loading the correct user keys into the FMPKEY control register. The protection keys on the A64 are located in the last 4 words of the first 8K sector. For more detailed information on the flash protection keys and the FMPKEY control register, see the protection keys portions of the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

flash read

The A64 flash memory is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The flash is addressed through memory selects 0 and 1.

NOTE:

> The flash external pump voltage (VCCP) is required for all operations (program, erase, and read).

flash pipeline mode

When in pipeline mode, the flash operates with a system clock frequency of up to 48 MHz. When in normal mode, the flash operates with a system clock frequency of up to 24 MHz). Flash in pipeline mode is capable of accessing 64-bit words and provides two 32-bit pipelined words to the CPU. Also in pipeline mode, the flash can be read with no wait states when memory addresses are contiguous (after the initial 1-or 2-wait-state reads).

NOTE:

> After a system reset, pipeline mode is **disabled** (the ENPIPE bit FMREGOPT[0] = 0). In other words, the A64 device powers up and comes out of reset in non-pipeline mode. Furthermore, setting the flash configuration mode bit (GLBCTRL[4]) will override pipeline mode.

flash program and erase

The A64 device flash has one 64K-byte bank that consists of five sectors. These five sectors are shown in Table 4.

Table 4. Flash Sectors

SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS
0	8K Bytes	0x0000_0000	0x0000_1FFF
1	8K Bytes	0x0000_2000	0x0000_3FFF
2	16K Bytes	0x0000_4000	0x0000_7FFF
3	16K Bytes	0x0000_8000	0x0000_BFFF
4	16K Bytes	0x0000_C000	0x0000_FFFF

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 16-bit word.

NOTE:

> The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

Execution can occur from one bank while programming/erasing any or all sectors of another bank. However, execution cannot occur from any sector within a bank that is being programmed or erased.

NOTE:

> When the OTP sector is enabled, the rest of the flash memory is disabled. The OTP memory can only be read or programmed from code executed out of RAM.

For more detailed information on flash program and erase operations, see the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

HET RAM

The A64 device contains HET RAM. The HET RAM has a 64-instruction capability. The HET RAM is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The HET RAM is addressed through memory select 4.

Peripheral Selects and Base Addresses

The A64 device uses 10 of the 16 peripheral selects to decode the base addresses of the peripherals. These peripheral selects are fixed and transparent to the user since they are part of the decoding scheme used by the SYS module.

Control registers for the peripherals, SYS module, and flash begin at the base addresses shown in Table 5.

Table 5. A64 Peripherals, System Module, and Flash Base Addresses

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
SYSTEM	0xFFFF_FD00	0xFFFF_FFFF	N/A
RESERVED	0xFFF8_0000	0xFFFF_FCFF	N/A
HET	0xFFF7_FC00	0xFFF7_FFFF	PS[0]
SPI1	0xFFF7_F800	0xFFF7_FBFF	PS[1]
SCI2	0XFFF7_F500	0XFFF7_F7FF	PS[2]
SCI1	0xFFF7_F400	0xFFF7_F4FF	
ADC	0xFFF7_F000	0xFFF7_F3FF	PS[3]
GIO/ECP	0xFFF7_EC00	0xFFF7_EFFF	PS[4]
Reserved	0xFFF7_E400	0xFFF7_EBFF	PS[5]–PS[6]
SCC	0xFFF7_E000	0xFFF7_E3FF	PS[7]
SCC RAM	0xFFF7_DC00	0xFFF7_DFFF	PS[8]
Reserved	0XFFF7_D800	0XFFF7_DBFF	PS[9]
SPI2	0XFFF7_D400	0XFFF7_D7FF	PS[10]
Reserved	0xFFF7_CC00	0xFFF7_D3FF	PS[11]–PS[12]
C2SIa	0xFFF7_C800	0xFFF7_CBFF	PS[13]
Reserved	0xFFF7_C000	0xFFF7_C7FF	PS[14]–PS[15]
Reserved	0xFFF0_0000	0xFFF7_BFFF	N/A
Flash control registers	0xFFE8_8000	0xFFE8_BFFF	N/A
MPU control registers	0xFFE8_4000	0xFFE8_4023	N/A

Interrupt Priority

The central interrupt manager (CIM) portion of the SYS module manages the interrupt requests from the device modules (i.e., SPI1 or SPI2, SCI1 or SCI2, and RTI, etc.).

Although the CIM can accept up to 32 interrupt request signals, the A64 device only uses 21 of those interrupt request signals. The request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the CIM to be of either type:

- Fast interrupt request (FIQ)
- Normal interrupt request (IRQ)

The precedences of request channels decrease with ascending channel order in the CIM (0, highest, and 31, lowest, priority). For these channel priorities and the associated modules, see Table 6.

Table 6. Interrupt Priority

MODULES	INTERRUPT SOURCES	INTERRUPT LEVEL/CHANNEL
SPI1	SPI1 end-transfer/overrun	0
RTI	COMP2 interrupt	1
RTI	COMP1 interrupt	2
RTI	TAP interrupt	3
SPI2	SPI2 end-transfer/overrun	4
GIO	Interrupt A	5
Reserved		6
HET	Interrupt A	7
Reserved		8
SCI1/SCI2	SCI1/SCI2 error interrupt	9
SCI1	SCI1 receive interrupt	10
C2SIa	C2SIa interrupt	11
Reserved		12
Reserved		13
SCC	Interrupt A	14
Reserved		15
MibADC	End event conversion	16
SCI2	SCI2 receive interrupt	17
Reserved		18
Reserved		19
SCI1	SCI1 transmit interrupt	20
System	SW interrupt (SSI)	21
Reserved		22
HET	Interrupt B	23
Reserved		24
SCC	Interrupt B	25
SCI2	SCI2 transmit interrupt	26
MibADC	End Group 1 conversion	27
Reserved		28
GIO	Interrupt B	29
MibADC	End Group 2 conversion	30
Reserved		31

MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The A64 MibADC module can function in two modes: compatibility mode, where its programmer's model is compatible with the TMS470R1x ADC module and its digital results are stored in digital result registers; or in buffered mode, where the digital result registers are replaced with three FIFO buffers, one for each conversion group (event, group1 [G1], and group2 [G2]). In buffered mode, the MibADC buffers can be serviced by interrupts.

MibADC event trigger enhancements

The MibADC includes two major enhancements over the event-triggering capability of the TMS470R1x ADC.

- Both group1 and the event group can be configured for event-triggered operation, providing up to two event-triggered groups.
- The trigger source and polarity can be selected individually for both group1 and the event group from the three options identified in Table 7.

Table 7. MibADC Event Hookup Configuration

EVENT #	SOURCE SELECT BITS FOR G1 OR EVENT (G1SRC[1:0] or EVSRC[1:0])	SIGNAL PIN NAME
EVENT1	00	ADEVT
EVENT2	01	HET18
EVENT3	10	HET19
EVENT4	11	Reserved

For group 1, these event-triggered selections are configured via the group1 source select bits (G1SRC[1:0]) in the AD event source register (ADEVTSRC[5:4]). For the event group, these event-triggered selections are configured via the event group source select bits (EVSRC[1:0]) in the AD event source register (ADEVTSRC[1:0]).

For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

Documentation Support

Extensive documentation supports all of the TMS470 microcontroller family generation of devices. The types of documentation available include: data sheets with design specifications; complete user's guides; and errata sheets. Useful reference documentation includes:

- Bulletin
  - *TMS470 Microcontroller Family Product Bulletin* (literature number SPNB086)
- User's Guides
  - *TMS470R1x System Module Reference Guide* (literature number SPNU189)
  - *TMS470R1x General-Purpose Input/Output (GIO) Reference Guide* (literature number SPNU192)
  - *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194)
  - *TMS470R1x Serial Peripheral Interface (SPI) Reference Guide* (literature number SPNU195)
  - *TMS470R1x Serial Communication Interface (SCI) Reference Guide* (literature number SPNU196)
  - *TMS470R1x Controller Area Network (CAN) Reference Guide* (literature number SPNU197)
  - *TMS470R1x High End Timer (HET) Reference Guide* (literature number SPNU199)
  - *TMS470R1x External Clock Prescale (ECP) Reference Guide* (literature number SPNU202)
  - *TMS470R1x MultiBuffered AnalogtoDigital (MibADC) Reference Guide* (literature number SPNU206)
  - *TMS470R1x ZeroPin PhaseLocked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212)
  - *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213)
  - *TMS470R1x Class II Serial Interface B (C2SIb) Reference Guide* (literature number SPNU214)
  - *TMS470R1x Class II Serial Interface A (C2SIa) Reference Guide* (literature number SPNU218)
  - *TMS470R1x Inter-Integrated Circuit (I2C) Reference Guide* (literature number SPNU223)
  - *TMS470 Peripherals Overview Reference Guide* (literature number SPNU248)
- Errata Sheet:
  - *TMS470R1A64 TMS470 Microcontrollers Silicon Errata* (literature number SPNZ134)

Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**470R1A64). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX	Experimental device that is not necessarily representative of the final device's electrical specifications
TMP	Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
TMS	Fully qualified production device

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing.
TMDS	Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

Figure 2 illustrates the numbering and symbol nomenclature for the TMS470R1x family.

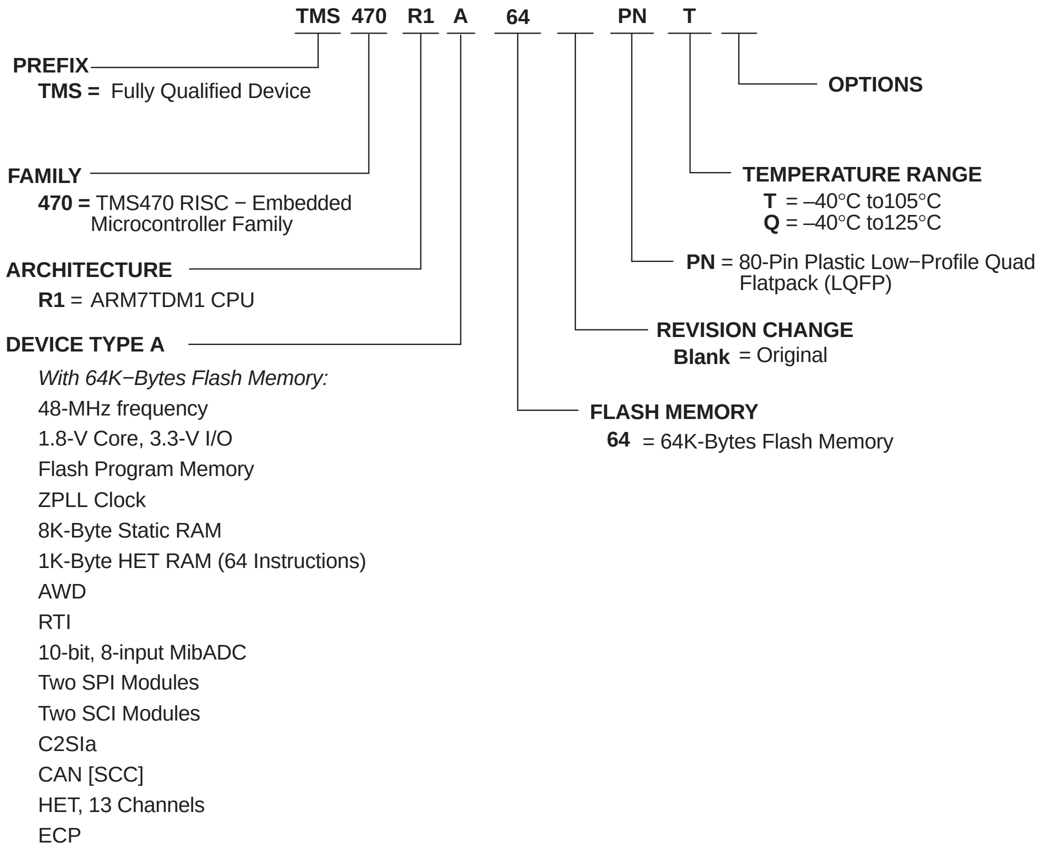


Figure 2. TMS470R1x Family Nomenclature

Device Identification Code Register

The device identification code register identifies the silicon version, the technology family (TF), a ROM or flash device, and an assigned device-specific part number (see Figure 3 and Table 8). The A64 device identification code register value is 0xn83F.

Figure 3. TMS470 Device ID Bit Allocation Register [offset = FFFF_FFF0]

31 16
Reserved

15 12	11	10	9 3	2	1	0
VERSION	TF	R/F	PART NUMBER	1	1	1
R-K	R-K	R-K	R-K	R-1	R-1	R-1

LEGEND: R = Read only; -K = value constant after $\overline{\text{RESET}}$; -1 = value after $\overline{\text{RESET}}$

Table 8. TMS470 Device ID Bit Allocation Register Description

BIT	NAME	Value	DESCRIPTION
31–16	Reserved		Reads are undefined and writes have no effect.
15–12	VERSION		Silicon version (revision) These bits identify the silicon version of the device.
11	TF		Technology Family This bit distinguishes the technology family core power supply:
		0	3.3 V for F10/C10 devices
		1	1.8 V for F05/C05 devices
10	R/F		ROM/Flash This bit distinguishes between ROM and flash devices:
		0	Flash device
		1	ROM device
9–3	PART NUMBER		Device-specific part number These bits identify the assigned device-specific part number. The assigned device-specific part number for the A64 device is 0000111.
2–0	1		Mandatory High Bits 2,1, and 0 are tied high by default.

DEVICE ELECTRICAL SPECIFICATIONS AND TIMING PARAMETERS

Absolute Maximum Ratings

Over operating free-air temperature range, T version unless otherwise noted[1]

Supply voltage range:	V_{CC} [2]	–0.5 V to 2.5 V
Supply voltage range:	V_{CCIO}, V_{CCAD}, V_{CCP} (flash pump)[2]	–0.5 V to 4.1 V
Input voltage range:	All input pins	–0.5 V to 4.1 V
Input clamp current:	I_{IK} ($V_I < 0$ or $V_I > V_{CCIO}$) All pins except ADIN[0:11], $\overline{\text{PORRST}}$, $\overline{\text{TRST}}$, TEST and TCK	± 20 mA
	I_{IK} ($V_I < 0$ or $V_I > V_{CCAD}$) ADIN[0:11]	±10 mA
Operating free-air temperature range, T_A:	T version	–40°C to 105°C
	Q version	–40°C to 125°C
Operating junction temperature range, T_J		–40°C to 150°C
Storage temperature range, T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to their associated grounds.

Device Recommended Operating Conditions[1]

			MIN	NOM	MAX	UNIT
V_{CC}	Digital logic and flash supply voltage (Core)		1.71		2.05	V
V_{CCIO}	Digital logic supply voltage (I/O)		3	3.3	3.6	V
V_{CCAD}	ADC supply voltage		3	3.3	3.6	V
V_{CCP}	flash pump supply voltage		3	3.3	3.6	V
V_{SS}	Digital logic supply ground			0		V
V_{SSAD}	ADC supply ground		–0.1		0.1	V
T_A	Operating free-air temperature	T version	–40		105	°C
		Q version	–40		125	
T_J	Operating junction temperature		–40		150	°C

(1) All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}.

Electrical Characteristics over Recommended Operating Free-Air Temperature Range(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis			0.15			V
V_{IL}	Low-level input voltage	All inputs(2) except OSCIN		–0.3		0.8	V
		OSCIN only		–0.3		$0.35V_{CC}$	
V_{IH}	High-level input voltage	All inputs except OSCIN		2		V_{CCIO} + 0.3	V
				$0.65V_{CC}$		V_{CC} + 0.3	
V_{th}	Input threshold voltage	AWD only		1.35		1.8	V
RDS_{ON}	Drain to source on resistance	AWD only(3)	V_{OL} = 0.35 V @ I_{OL} = 8 mA			45	Ω
V_{OL}	Low-level output voltage(4)		$I_{OL} = I_{OL}$ MAX			0.2 V_{CCIO}	V
			I_{OL} = 50 µA			0.2	
V_{OH}	High-level output voltage(4)		$I_{OH} = I_{OH}$ MIN	0.8 V_{CCIO}			V
			I_{OH} = 50 µA	V_{CCIO} – 0 .2			
I_{IC}	Input clamp current (I/O pins)(5)		$V_I < V_{SSIO}$ – 0. 3 or $V_I > V_{CCIO}$ + 0. 3	–2		2	mA
I_I	Input current (I/O pins)	I_{IL} Pulldown	$V_I = V_{SS}$	–1		1	µA
		I_{IH} Pulldown	$V_I = V_{CCIO}$	5		40	
		I_{IL} Pullup	$V_I = V_{SS}$	–40		–5	
		I_{IH} Pullup	$V_I = V_{CCIO}$	–1		1	
		All other pins	No pullup or pulldown	–1		1	
I_{OL}	Low-level output current	CLKOUT, AWD, TDO	$V_{OL} = V_{OL}$ MAX			8	mA
		$\overline{\text{RST}}$, SPI1CLK, SPI1SOMI, SPI1SIMO, SPI2CLK, SPI2SOMI, SPI2SIMO	$V_{OL} = V_{OL}$ MAX			4	
		All other output pins(6)	$V_{OL} = V_{OL}$ MAX			2	
I_{OH}	High-level output current	CLKOUT, TDO	$V_{OH} = V_{OH}$ MIN	–8			mA
		SPI1CLK, SPI1SOMI, SPI1SIMO, SPI2CLK, SPI2SOMI, SPI2SIMO	$V_{OH} = V_{OH}$ MIN	–4			
		All other output pins except $\overline{\text{RST}}$(6)	$V_{OH} = V_{OH}$ MIN	–2			
I_{CC}	V_{CC} Digital supply current (operating mode)		SYSCLK = 48 MHz, ICLK = 24 MHz, V_{CC} = 2.05 V			70	mA
	V_{CC} Digital supply current (standby mode)(7)		OSCIN = 6 MHz, V_{CC} = 2.06 V			3.0	mA
	V_{CC} Digital supply current (halt mode)(7)		V_{CC} = 2.06 V			1.0	mA

---

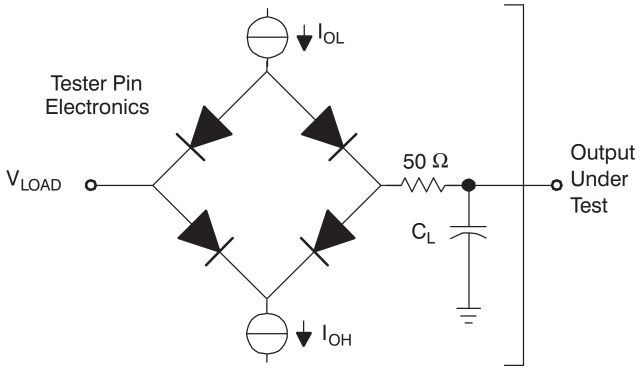
(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) This does not apply to the $\overline{\text{PORRST}}$ pin. For $\overline{\text{PORRST}}$ exceptions, see the $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ timings section.
(3) These values help to determine the external RC network circuit. For more details, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).
(4) V_{OL} and V_{OH} are linear with respect to the amount of load current (I_{OL}/I_{OH}) applied.
(5) Parameter does not apply to input-only or output-only pins.
(6) The 2 mA buffers on this device are called zero-dominant buffers. If two of these buffers are shorted together and one is outputting a low level and the other is outputting a high level, the resulting value will always be low.
(7) For flash banks/pumps in sleep mode.

Electrical Characteristics over Recommended Operating Free-Air Temperature Range (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCIO}	V_{CCIO} Digital supply current (operating mode)	No DC load, V_{CCIO} = 3.6 V(8)			10	mA
	V_{CCIO} Digital supply current (standby mode)	No DC load, V_{CCIO} = 3.6 V(8)			300	µA
	V_{CCIO} Digital supply current (halt mode)	No DC load, V_{CCIO} = 3.6 V(8)			300	µA
I_{CCAD}	V_{CCAD} supply current (operating mode)	All frequencies, V_{CCAD} = 3.6 V			15	mA
	V_{CCAD} supply current (standby mode)	All frequencies, V_{CCAD} = 3.6 V			20	µA
	V_{CCAD} supply current (halt mode)	All frequencies, V_{CCAD} = 3.6 V			20	µA
I_{CCP}	V_{CCP} pump supply current	V_{CCP} = 3.6 V read operation			50	mA
		V_{CCP} = 3.6 V program and erase			70	mA
		V_{CCP} = 3.6 V standby mode operation(7)			20	µA
		V_{CCP} = 3.6 V halt mode operation(7)			20	µA
C_I	Input capacitance			2		pF
C_O	Output capacitance			3		pF

(8) I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} - 0.2 V.

Parameter Measurement Information



Where: I_{OL} = I_{OL} MAX for the respective pin (A)
I_{OH} = I_{OH} MIN for the respective pin(A)
V_{LOAD} = 1.5 V
C_L = 150-pF typical load-circuit capacitance(B)

A. For these values, see the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.

B. All timing parameters measured using an external load capacitance of 150 pF unless otherwise noted.

Figure 4. Test Load Circuit

Timing Parameter Symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

CM	Compaction, CMPCT	RD	Read
CO	CLKOUT	RST	Reset, $\overline{\text{RST}}$
ER	Erase	RX	SCInRX
ICLK	Interface clock	S	Slave mode
M	Master mode	SCC	SCInCLK
OSC, OSCI	OSCIN	SIMO	SPInSIMO
OSCO	OSCOUT	SOMI	SPInSOMI
P	Program, PROG	SPC	SPInCLK
R	Ready	SYS	System clock
R0	Read margin 0, RDMRGN0	TX	SCInTX
R1	Read margin 1, RDMRGN1		

Lowercase subscripts and their meanings are:

a	access time	r	rise time
c	cycle time (period)	su	setup time
d	delay time	t	transition time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

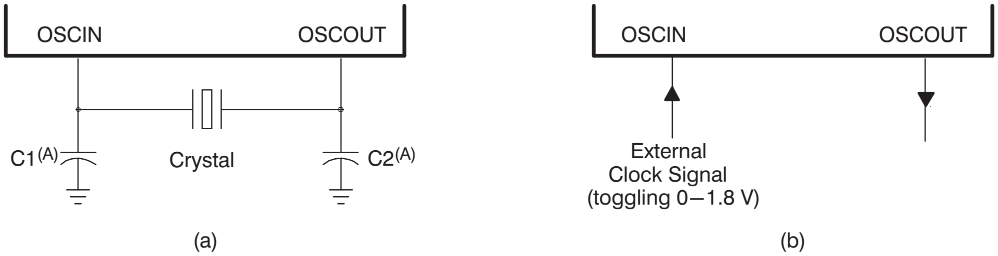
The following additional letters are used with these meanings:

H	High	X	Unknown, changing, or don't care level
L	Low	Z	High impedance
V	Valid		

External Reference Resonator/Crystal Oscillator Clock Option

The oscillator is enabled by connecting the appropriate fundamental 4–20 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 5a. The oscillator is a single-stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode. **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation.** The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 1.8-V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 5b.



(a)

(b)

A. The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 5. Crystal/Clock Connection

ZPLL AND CLOCK SPECIFICATIONS

Timing Requirements for ZPLL Circuits Enabled or Disabled

		MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Input clock frequency	4		20	MHz
$t_{c(OSC)}$	Cycle time, OSCIN	50			ns
$t_{w(OSCIL)}$	Pulse duration, OSCIN low	15			ns
$t_{w(OSCIH)}$	Pulse duration, OSCIN high	15			ns
$f_{(OSCRST)}$	OSC FAIL frequency(1)		53		kHz

(1) Causes a device reset (specifically a clock reset) by setting the RST OSC FAIL (GLBCTRL[15]) and the OSC FAIL flag (GLBSTAT[1]) bits equal to 1. For more detailed information on these bits and device resets, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

Switching Characteristics over Recommended Operating Conditions for Clocks(1)(2)

PARAMETER		TEST CONDITIONS(3)	MIN	MAX	UNIT
$f_{(SYS)}$	System clock frequency(4)	Pipeline mode enabled		48	MHz
		Pipeline mode disabled		24	
$f_{(CONFIG)}$	System clock frequency - flash config mode			24	MHz
$f_{(ICLK)}$	Interface clock frequency	Pipeline mode enabled		25	MHz
		Pipeline mode disabled		24	
$f_{(ECLK)}$	External clock output frequency for ECP Module	Pipeline mode enabled		25	MHz
		Pipeline mode disabled		24	
$t_{c(SYS)}$	Cycle time, system clock	Pipeline mode enabled	20.8		ns
		Pipeline mode disabled	41.6		
$t_{c(CONFIG)}$	Cycle time, system clock - flash config mode		41.6		ns
$t_{c(ICLK)}$	Cycle time, interface clock	Pipeline mode enabled	40		ns
		Pipeline mode disabled	41.6		
$t_{c(ECLK)}$	Cycle time, ECP module external clock output	Pipeline mode enabled	40		ns
		Pipeline mode disabled	41.6		

(1) $f_{(SYS)} = M \times f_{(OSC)}/R$, where M = {4 or 8}, R = {1,2,3,4,5,6,7,8} when PLLDIS = 0. R is the system-clock divider determined by the CLKDIVPRE [2:0] bits in the global control register (GLBCTRL[2:0]) and M is the PLL multiplier determined by the MULT4 bit also in the GLBCTRL register (GLBCTRL.3).
$f_{(SYS)} = f_{(OSC)}/R$, where R = {1,2,3,4,5,6,7,8} when PLLDIS = 1.
$f_{(ICLK)} = f_{(SYS)}/X$, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.

(2) $f_{(ECLK)} = f_{(ICLK)}/N$, where N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.

(3) Pipeline mode enabled or disabled is determined by the ENPIPE bit (FMREGOPT[0]).

(4) Flash Vread must be set to 5V to achieve maximum system clock frequency.

Switching Characteristics over Recommended Operating Conditions for External Clocks[(1)][(2)][(3)]

(See Figure 6 and Figure 7)

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
$t_{w(COL)}$	Pulse duration, CLKOUT low	SYSCLK or MCLK`(4)	$0.5t_{c(SYS)} – t_f$		ns
		ICLK, X is even or 1(5)	$0.5t_{c(ICLK)} – t_f$		
		ICLK, X is odd and not 1(5)	$0.5t_{c(ICLK)} + 0.5t_{c(SYS)} – t_f$		
$t_{w(COH)}$	Pulse duration, CLKOUT high	SYSCLK or MCLK(4)	$0.5t_{c(SYS)} – t_r$		ns
		ICLK, X is even or 1(5)	$0.5t_{c(ICLK)}$ – tr		
		ICLK, X is odd and not 1(5)	$0.5t_{c(ICLK)} – 0.5t_{c(SYS)} – t_r$		
$t_{w(EOL)}$	Pulse duration, ECLK low	N is even and X is even or odd	$0.5t_{c(ECLK)} – t_f$		ns
		N is odd and X is even	$0.5t_{c(ECLK)} – t_f$		
		N is odd and X is odd and not 1	$0.5t_{c(ECLK)} + 0.5t_{c(SYS)} – t_f$		
$t_{w(EOH)}$	Pulse duration, ECLK high	N is even and X is even or odd	$0.5t_{c(ECLK)} – t_r$		ns
		N is odd and X is even	$0.5t_{c(ECLK)} – t_r$		
		N is odd and X is odd and not 1	$0.5t_{c(ECLK)} – 0.5t_{c(SYS)} – t_r$		

(1) X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.
(2) N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.
(3) CLKOUT/ECLK pulse durations (low/high) are a function of the OSCIN pulse durations when PLLDIS is active.
(4) Clock source bits selected as either SYSCLK (CLKCNTL[6:5] = 11 binary) or MCLK (CLKCNTL[6:5] = 10 binary).
(5) Clock source bits selected as ICLK (CLKCNTL[6:5] = 01 binary).

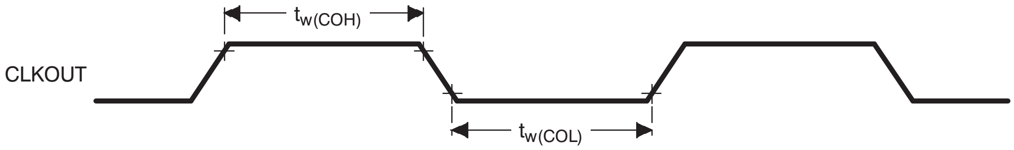


Figure 6. CLKOUT Timing Diagram

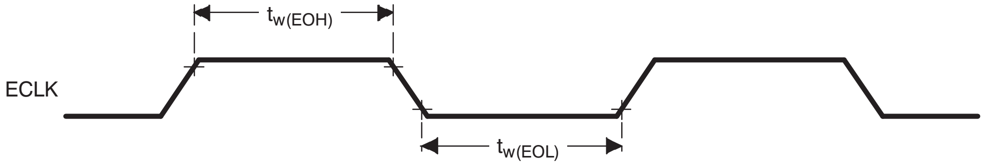


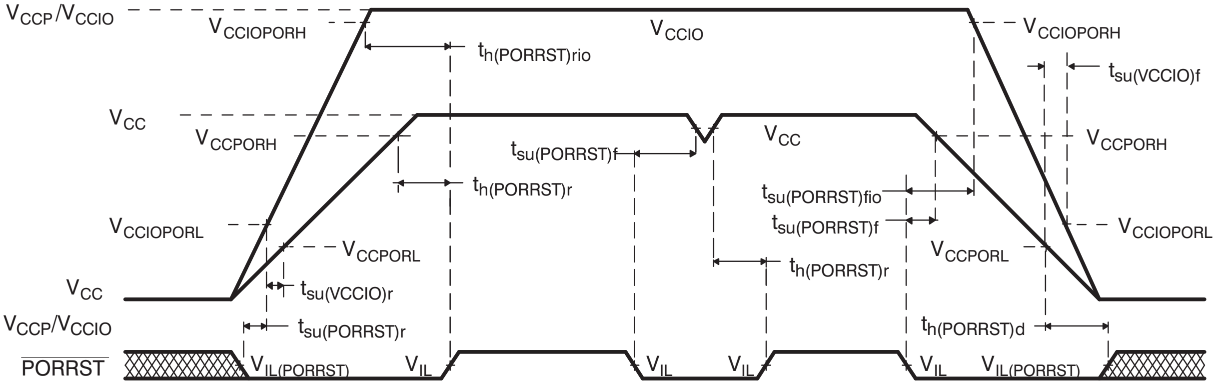
Figure 7. ECLK Timing Diagram

$\overline{\text{RST}}$ AND $\overline{\text{PORRST}}$ TIMINGS

Timing Requirements for $\overline{\text{PORRST}}$

(see Figure 8)

		MIN	MAX	UNIT
V_{CCPORL}	V_{CC} low supply level when $\overline{\text{PORRST}}$ must be active during power up		0.6	V
V_{CCPORH}	V_{CC} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	1.5		V
$V_{CCIOPORL}$	V_{CCIO} low supply level when $\overline{\text{PORRST}}$ must be active during power up		1.1	V
$V_{CCIOPORH}$	V_{CCIO} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	2.75		V
V_{IL}	Low-level input voltage after $V_{CCIO} > V_{CCIOPORH}$		$0.2V_{CCIO}$	V
$V_{IL(PORRST)}$	Low-level input voltage of $\overline{\text{PORRST}}$ before $V_{CCIO} > V_{CCIOPORL}$		0.5	V
$t_{su(PORRST)r}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CCIO} > V_{CCIOPORL}$ during power up	0		ms
$t_{su(VCCIO)r}$	Setup time, $V_{CCIO} > V_{CCIOPORL}$ before $V_{CC} > V_{CCPORL}$	0		ms
$t_{h(PORRST)r}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCPORH}$	1		ms
$t_{su(PORRST)f}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCPORH}$ during power down	8		ms
$t_{h(PORRST)rio}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCIOPORH}$	1		ms
$t_{h(PORRST)d}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} < V_{CCPORL}$	0		ms
$t_{su(PORRST)fio}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCIOPORH}$ during power down	0		ms
$t_{su(VCCIO)f}$	Setup time, $V_{CC} < V_{CCPORL}$ before $V_{CCIO} < V_{CCIOPORL}$	0		ms



NOTE: V_{CCIO} > 1.1 V before V_{CC} > 0.6 V

Figure 8. $\overline{\text{PORRST}}$ Timing Diagram

Switching Characteristics over Recommended Operating Conditions for $\overline{RST}$ (1)

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, $\overline{RST}$ active after PORRST inactive	$4112t_{c(OSC)}$		ns
	Valid time, $\overline{RST}$ active (all others)	$8t_{c(SYS)}$		
T_{fsu}	Flash start-up time, from $\overline{RST}$ inactive to fetch of first instruction from flash (flash pump stabilization time)	$336t_{c(OSC)}$		ns

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.

JTAG SCAN INTERFACE TIMING

(JTAG clock specification 10-MHz and 50-pF load on TDO output)

		MIN	MAX	UNIT
$t_{c(JTAG)}$	Cycle time, JTAG low and high period	50		ns
$t_{su(TDI/TMS\text{ - }TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	15		ns
$t_{h(TCKr\text{ -}TDI/TMS)}$	Hold time, TDI, TMS after TCKr	15		ns
$t_{h(TCKf\text{ -}TDO)}$	Hold time, TDO after TCKf	10		ns
$t_{d(TCKf\text{ -}TDO)}$	Delay time, TDO valid after TCK fall (TCKf)		45	ns

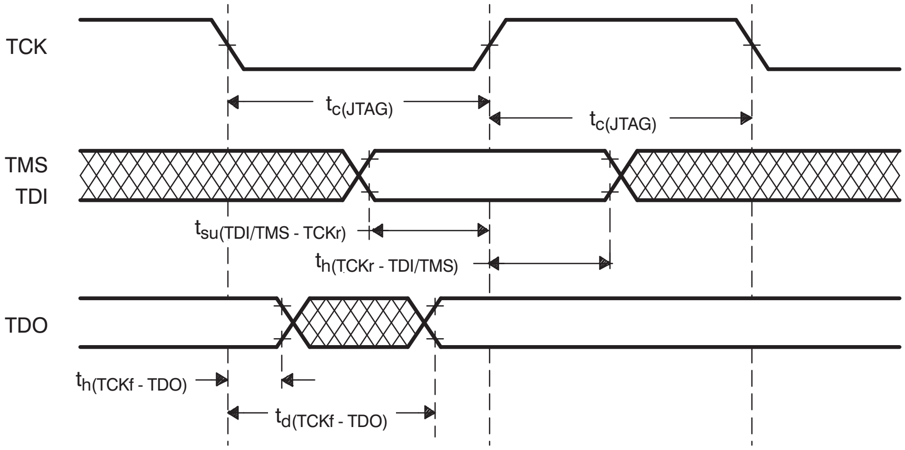


Figure 9. JTAG Scan Timings

OUTPUT TIMINGS

Switching Characteristics for Output Timings versus Load Capacitance ©$_L$)

(See Figure 10)

PARAMETER			MIN	MAX	UNIT
t_r	Rise time, CLKOUT, AWD, TDO	C_L = 15 pF	0.5	2.50	ns
		C_L = 50 pF	1.5	5	
		C_L = 100 pF	3	9	
		C_L = 150 pF	4.5	12.5	
t_f	Fall time, CLKOUT, AWD, TDO	C_L = 15 pF	0.5	2.5	ns
		C_L = 50 pF	1.5	5	
		C_L = 100 pF	3	9	
		C_L = 150 pF	4.5	12.5	
t_r	Rise time, SPI1CLK, SPI1SOMI, SPI1SIMO, SPI2CLK, SPI2SOMI, SPI2SIMO	C_L = 15 pF	2.5	8	ns
		C_L = 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_f	Fall time, $\overline{\text{RST}}$, SPI1CLK, SPI1SOMI, SPI1SIMO, SPI2CLK, SPI2SOMI, SPI2SIMO	C_L = 15 pF	2.5	8	ns
		C_L = 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_r	Rise time, all other output pins	C_L = 15 pF	2.5	10	ns
		C_L = 50 pF	6.0	25	
		C_L = 100 pF	12	45	
		C_L = 150 pF	18	65	
t_f	Fall time, all other output pins	C_L = 15 pF	3	10	ns
		C_L = 50 pF	8.5	25	
		C_L = 100 pF	16	45	
		C_L = 150 pF	23	65	

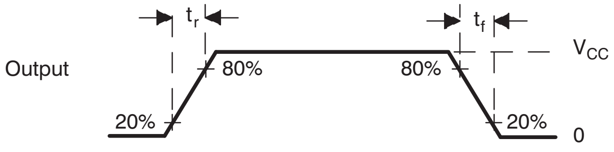


Figure 10. CMOS-Level Outputs

INPUT TIMINGS

Timing Requirements for Input Timings[1]

(See Figure 11)

		MIN	MAX	UNIT
t_{pw}	Input minimum pulse width	$t_{c(ICLK)}$ + 10		ns

[1] $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$

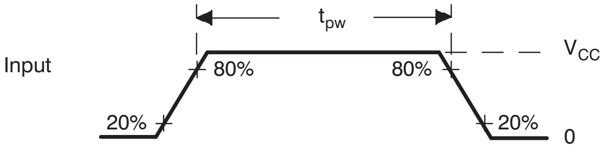


Figure 11. CMOS-Level Inputs

FLASH TIMINGS

Timing Requirements for Program Flash[1]

		MIN	TYP	MAX	UNIT
$t_{prog(16\text{-}bit)}$	Half word (16-bit) programming time	4	16	200	µs
$t_{prog(Total)}$	64K-byte programming time[2]		0.5	2	s
$t_{erase(sector)}$	Sector erase time		1.7		s
t_{wec}	Write/erase cycles at T_A = –40°C to 125°C	50000			cycles
$t_{fp(\overline{RST})}$	Flash pump settling time from $\overline{\text{RST}}$ to SLEEP		$67t_{c(SYS)}$		ns
$t_{fp(SLEEP)}$	Initial flash pump settling time from SLEEP to STANDBY		$67t_{c(SYS)}$		ns
$t_{fp(STANDBY)}$	Initial flash pump settling time from STANDBY to ACTIVE		$34t_{c(SYS)}$		ns

[1] For more detailed information on the flash core sectors, see the *Flash program and erase section* of this data sheet.
[2] The 64K-byte programming times include overhead of state machine.

SPIn MASTER MODE TIMING PARAMETERS

SPIn Master Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3) (see Figure 12)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK(4)	100	$256t_{c(ICLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4(5)	$t_{d(SPCH-SIMO)M}$	Delay time, SPInCLK high to SPInSIMO valid (clock polarity = 0)	0	10	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPInCLK low to SPInSIMO valid (clock polarity = 1)	0	10	
5(5)	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	$t_{c(SPC)M} - 5 - t_f$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	$t_{c(SPC)M} - 5 - t_r$		
6(5)	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 0)	6		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 1)	6		
7(5)	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 0)	4		ns
	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 1)	4		

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2[0]) is cleared.
(2) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) When the SPI is in master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

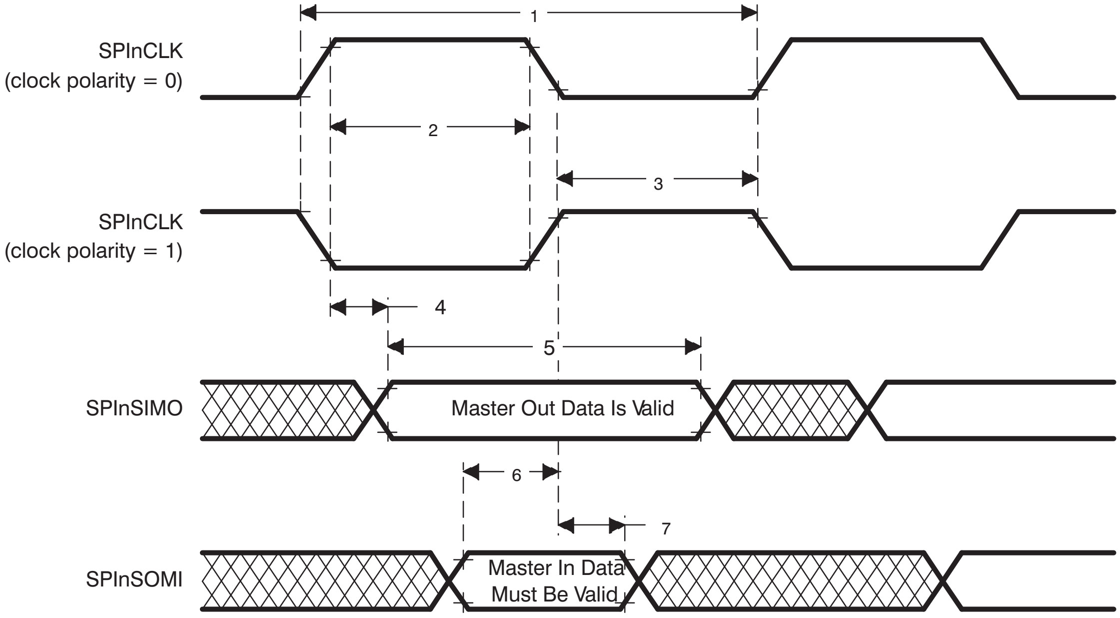


Figure 12. SPIn Master Mode External Timing (CLOCK PHASE = 0)

SPIn Master Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3) (see Figure 13)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK(4)	100	$256t_{c(ICLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4(5)	$t_{v(SIMO-SPCH)M}$	Valid time, SPInCLK high after SPInSIMO data valid (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		ns
	$t_{v(SIMO-SPCL)M}$	Valid time, SPInCLK low after SPInSIMO data valid (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		
5(6)	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	$t_{c(SPC)M} - 5 - t_f$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	$t_{c(SPC)M} - 5 - t_r$		
6(5)	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 0)	6		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 1)	6		
7(5)	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	4		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	4		

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2[0]) is set.
(2) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) When the SPI is in master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
(5) The active edge of the SPInCLK signal referenced is controlled by the clock polarity bit (SPInCTRL2[1]).
(6) The active edge of the SPInCLK signal referenced is controlled by the clock polarity bit (SPInCTRL2[1]).

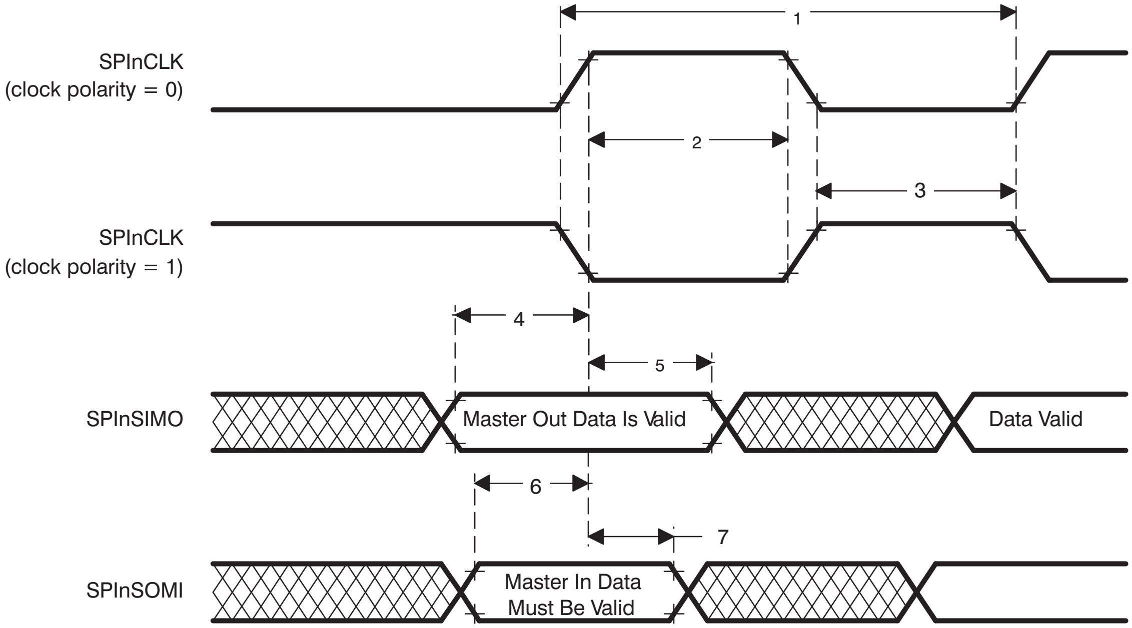


Figure 13. SPIn Master Mode External Timing (CLOCK PHASE = 1)

SPIn SLAVE MODE TIMING PARAMETERS

SPIn Slave Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4) (see Figure 14)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	100	$256t_{c(ICLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0)		$6 + t_r$	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1)		$6 + t_f$	
5(6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$t_{c(SPC)S} - 6 - t_r$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$t_{c(SPC)S} - 6 - t_f$		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 0)	6		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 1)	6		
7(6)	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	6		ns
	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	6		

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2[0]) is cleared.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1[12:5].
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
(5) When the SPIn is in slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the clock polarity bit (SPInCTRL2[1]).

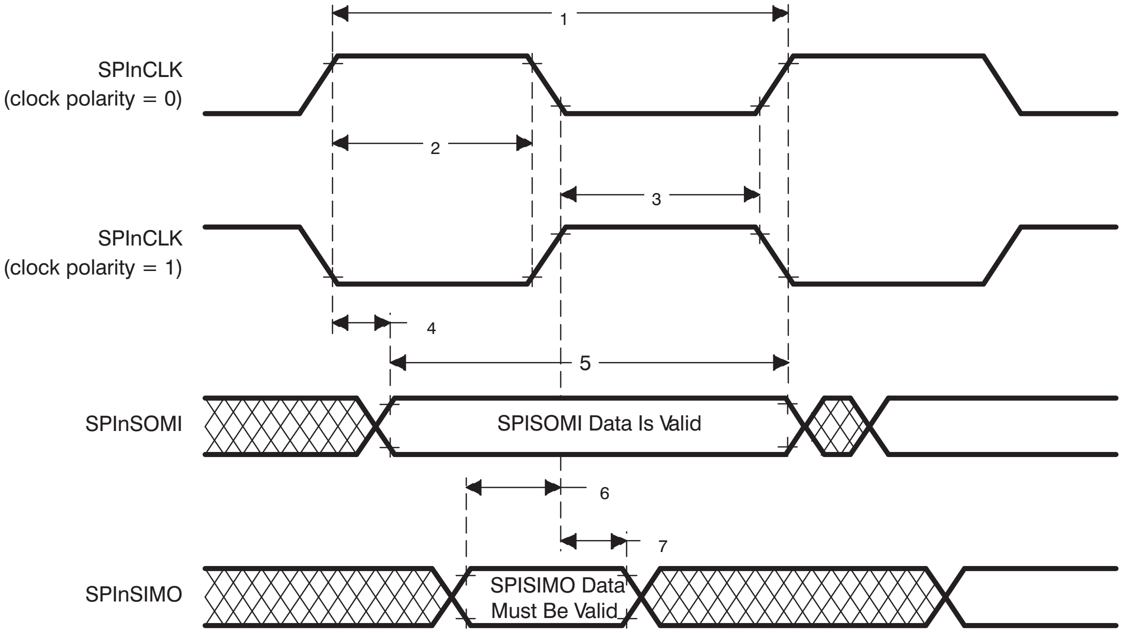


Figure 14. SPIn Slave Mode External Timing (CLOCK PHASE = 0)

SPIn Slave Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output) (1)(2)(3)(4) (see Figure 15)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK (5)	100	$256t_{c(ICLK)}$	ns
2 (6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
3 (6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
4 (6)	$t_{v(SOMI-SPCH)S}$	Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0)	$0.5t_{c(SPC)S} - 6 - t_r$		ns
	$t_{v(SOMI-SPCL)S}$	Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1)	$0.5t_{c(SPC)S} - 6 - t_f$		
5 (6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 6 - t_r$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 6 - t_f$		
6 (6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 0)	6		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 1)	6		
7 (6)	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	6		ns
	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	6		

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2[0]) is set.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\, t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1[12:5].
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
(5) When the SPIn is in slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the clock polarity bit (SPInCTRL2[1]).

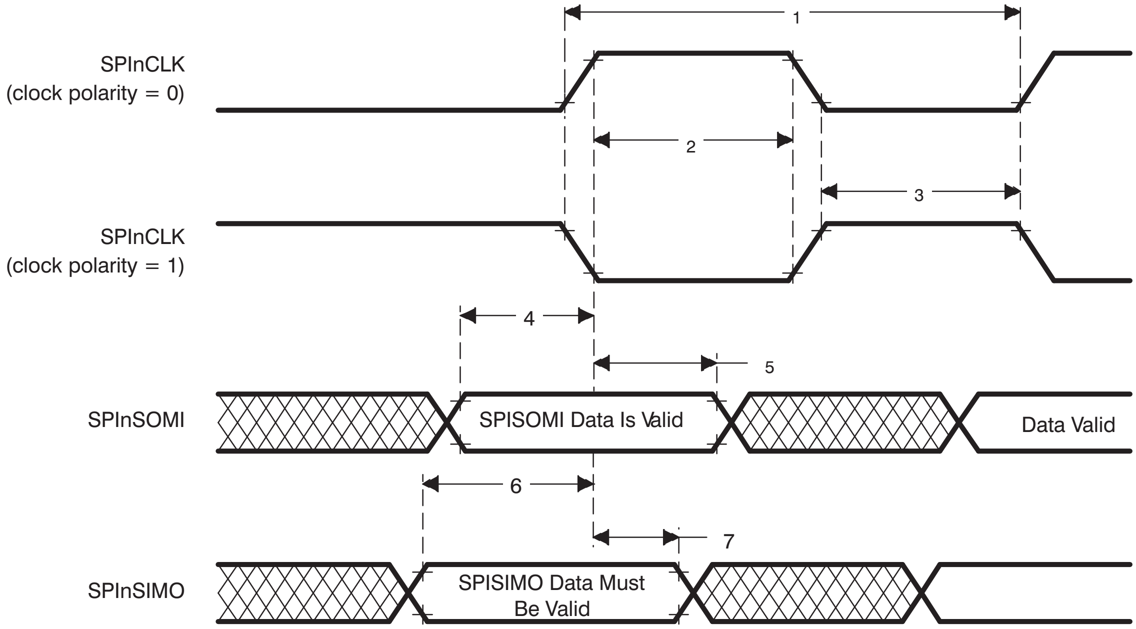


Figure 15. SPIn Slave Mode External Timing (CLOCK PHASE = 1)

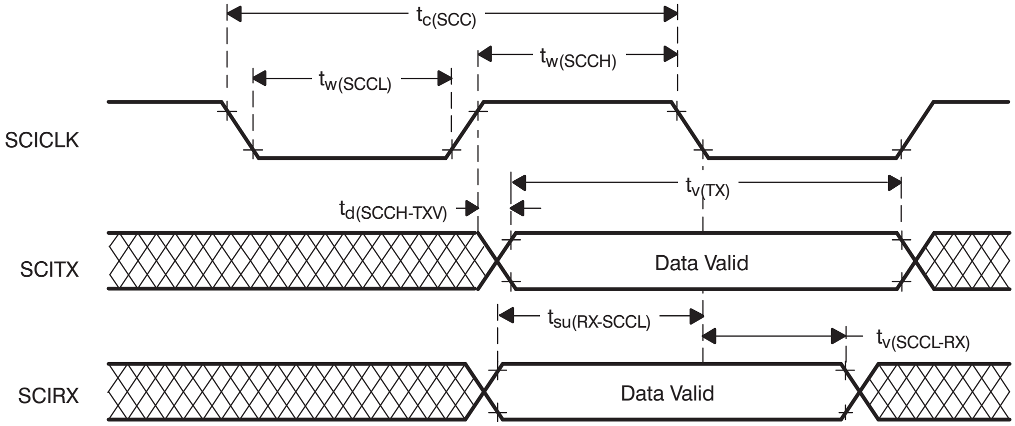
SCIn ISOSYNCHRONOUS MODE TIMINGS INTERNAL CLOCK

Timing Requirements for Internal Clock SCIn Isosynchronous Mode(1)(2)(3)

(see Figure 16)

		(BAUD + 1) IS EVEN OR BAUD = 0		(BAUD + 1) IS ODD AND BAUD ≠ 0		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCC)}$	Cycle time, SCInCLK	$2t_{c(ICLK)}$	$2^{24}\ t_{c(ICLK)}$	$3t_{c(ICLK)}$	$(2^{24}-1)\ t_{c(ICLK)}$	ns
$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - t_f$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)} - t_f$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)}$	ns
$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - t_r$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)} - t_r$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)}$	ns
$t_{d(SCCH-TXV)}$	Delay time, SCInCLK high to SCInTX valid		10		10	ns
$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$t_{c(SCC)} - 10$		$t_{c(SCC)} - 10$		ns
$t_{su(RX-SCCL)}$	Setup time, SCInRX before SCInCLK low	$t_{c(ICLK)} + t_f + 20$		$t_{c(ICLK)} + t_f + 20$		ns
$t_{v(SCCL-RX)}$	Valid time, SCInRX data after SCInCLK low	$-t_{c(ICLK)} + t_f + 20$		$-t_{c(ICLK)} + t_f + 20$		ns

(1) BAUD = 24-bit concatenated value formed by the SCI[H,M,L]BAUD registers.
(2) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table



A. Data transmission/reception characteristics for isosynchronous mode with internal clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception occurs on the SCICLK falling edge.

Figure 16. SCIn Isosynchronous Mode Timing Diagram for Internal Clock

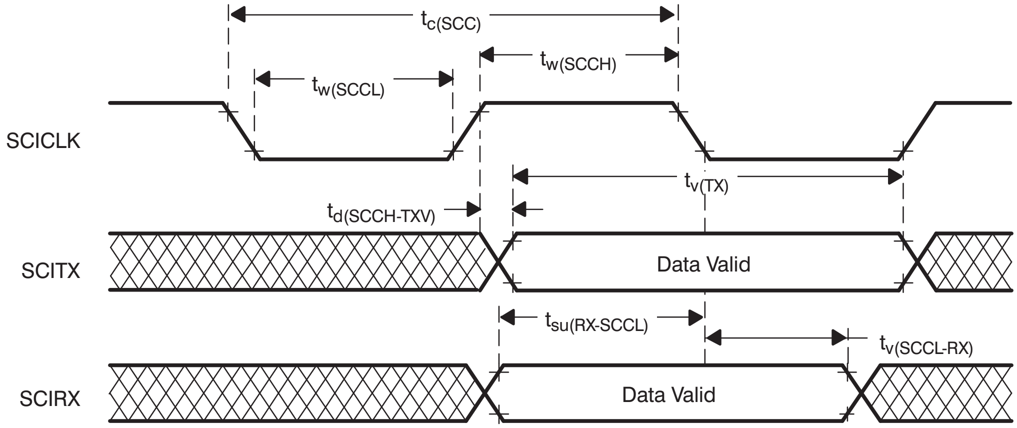
SCIn ISOSYNCHRONOUS MODE TIMINGS EXTERNAL CLOCK

Timing Requirements for External Clock SCIn Isosynchronous Mode(1)(2)

(see Figure 17)

		MIN	MAX	UNIT
$t_{c(SCC)}$	Cycle time, SCInCLK(3)	$8t_{c(ICLK)}$		ns
$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
$t_{d(SCCH-TXV)}$	Delay time, SCInCLK high to SCInTX valid		$2t_{c(ICLK)} + 12 + t_r$	ns
$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$2t_{c(SCC)} - 10$		ns
$t_{su(RX-SCCL)}$	Setup time, SCInRX before SCInCLK low	0		ns
$t_{v(SCCL-RX)}$	Valid time, SCInRX data after SCInCLK low	$2t_{c(ICLK)} + 10$		ns

(1) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
(2) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(3) When driving an external SCInCLK, the following must be true: $t_{c(SCC)} \geq 8t_{c(ICLK)}$



A. Data transmission / reception characteristics for isosynchronous mode with external clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception occurs on the SCICLK falling edge.

Figure 17. SCIn Isosynchronous Mode Timing Diagram for External Clock

HIGH-END TIMER (HET) TIMINGS

Minimum PWM Output Pulse Width:

This is equal to one high resolution clock period (HRP). The HRP is defined by the 6-bit high resolution prescale factor (hr), which is user defined, giving prescale factors of 1 to 64, with a linear increment of codes.

Therefore, the minimum PWM output pulse width = HRP(min) = hr(min)/SYSCLK = 1/SYSCLK

For example, for a SYSCLK of 30 MHz, the minimum PWM output pulse width = 1/30 = 33.33ns

Minimum Input Pulses that Can Be Captured:

The input pulse width must be greater or equal to the low resolution clock period (LRP), i.e., the HET loop (the HET program must fit within the LRP). The LRP is defined by the 3-bit loop-resolution prescale factor (lr), which is user defined, with a power of 2 increment of codes. That is, the value of lr can be 1, 2, 4, 8, 16, or 32.

Therefore, the minimum input pulse width = LRP(min) = hr(min) * lr(min)/SYSCLK = 1 * 1/SYSCLK

For example, with a SYSCLK of 30 MHz, the minimum input pulse width = 1 * 1/30 = 33.33 ns

NOTE:

> Once the input pulse width is greater than LRP, the resolution of the measurement is still HRP. (That is, the captured value gives the number of HRP clocks inside the pulse.)

Abbreviations:

hr = HET high resolution divide rate = 1, 2, 3,...63, 64

lr = HET low resolution divide rate = 1, 2, 4, 8, 16, 32

High resolution clock period = HRP = hr/SYSCLK

Loop resolution clock period = LRP = hr*lr/SYSCLK

STANDARD CAN CONTROLLER (SCC) MODE TIMINGS

Dynamic Characteristics for the CANSTX and CANSRX Pins

PARAMETER		MIN	MAX	UNIT
$t_{d(CANSTX)}$	Delay time, transmit shift register to CANSTX pin[1]		15	ns
$t_{d(CANSRX)}$	Delay time, CANSRX pin to receive shift register		5	ns

[1] These values do not include rise/fall times of the output buffer.

MULTI-BUFFERED A-TO-D CONVERTER (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry. This power bus enhances the A-to-D performance by preventing digital switching noise on the logic circuitry that could be present on V_{SS} and V_{CC} from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD_{REFLO} unless otherwise noted.

Resolution	10 bits (1024 values)
Monotonic	Assured
Output conversion code	00h to 3FFh [00 for $V_{AI} \leq AD_{REFLO}$; 3FF for $V_{AI} \geq AD_{REFHI}$]

MibADC Recommended Operating Conditions(1)

		MIN	MAX	UNIT
AD_{REFHI}	A-to-D high-voltage reference source	V_{SSAD}	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	V_{CCAD}	V
V_{AI}	Analog input voltage	$V_{SSAD} - 0.3$	$V_{CCAD} + 0.3$	V
I_{AIC}	Analog input clamp current(2) ($V_{AI} < V_{SSAD} - 0.3$ or $V_{AI} > V_{CCAD} + 0.3$)	–2	2	mA

(1) For V_{CCAD} and V_{SSAD} recommended operating conditions, see the "device recommended operating conditions" table.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

Operating Characteristics over Full Ranges of Recommended Operating Conditions(1)(2)

PARAMETER		DESCRIPTION/CONDITIONS		MIN	TYP	MAX	UNIT
R_I	Analog input resistance	See Figure 18.			250	500	Ω
C_I	Analog input capacitance	See Figure 18.	Conversion			10	pF
			Sampling			30	pF
I_{AIL}	Analog input leakage current	See Figure 18.		–1		1	µA
$I_{ADREFHI}$	AD_{REFHI} input current	$AD_{REFHI} = 3.6$ V, $AD_{REFLO} = V_{SSAD}$				5	mA
CR	Conversion range over which specified accuracy is maintained	$AD_{REFHI} - AD_{REFLO}$		3		3.6	V
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value after offset correction. See Figure 19.				±2	LSB
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error after offset correction. See Figure 20.				±2	LSB
E_{TOT}	Total error/Absolute accuracy	Maximum value of the difference between an analog value and the ideal midstep value. See Figure 21.				±2	LSB

(1) $V_{CCAD} = AD_{REFHI}$
(2) 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$ for the MibADC

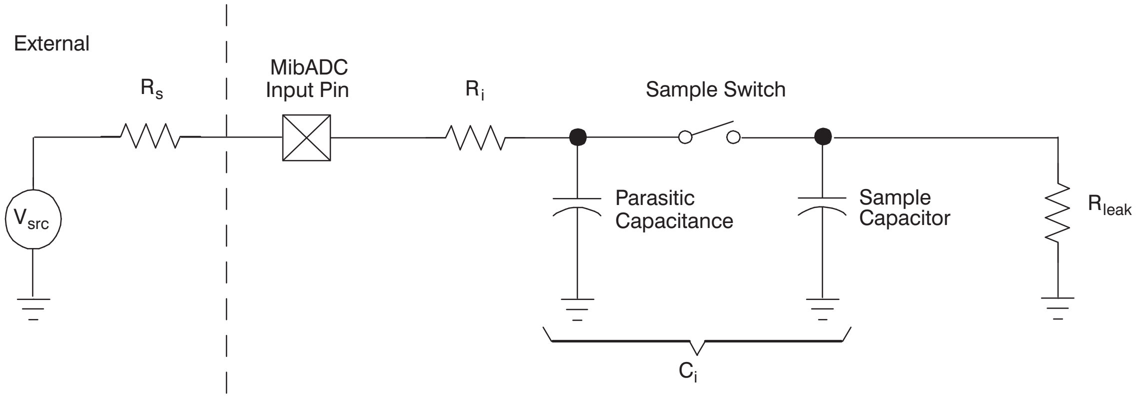


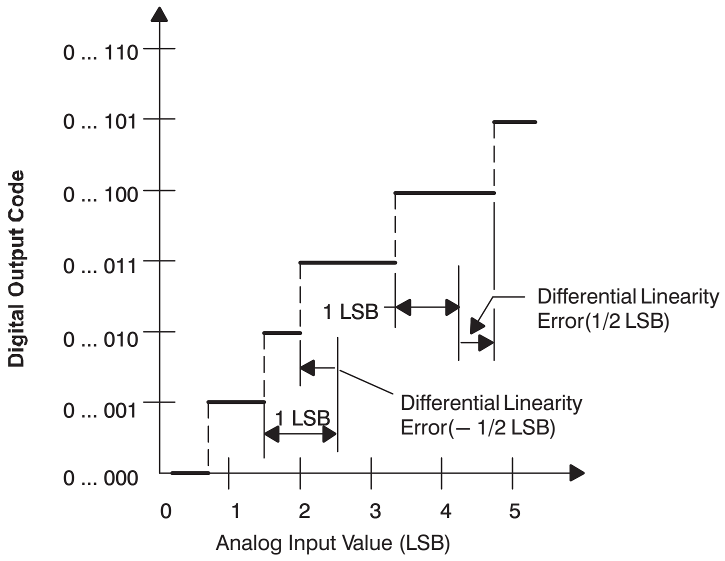
Figure 18. MibADC Input Equivalent Circuit

Multi-Buffer ADC Timing Requirements

		MIN	MAX	UNIT
$t_{c(ADCLK)}$	Cycle time, MibADC clock	0.05		µs
$t_{d(SH)}$	Delay time, sample and hold time	1		µs
$t_{d©)}$	Delay time, conversion time	0.55		µs
$t_{d(SHC)}$ (1)	Delay time, total sample/hold and conversion time	1.55		µs

(1) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors; for more details, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

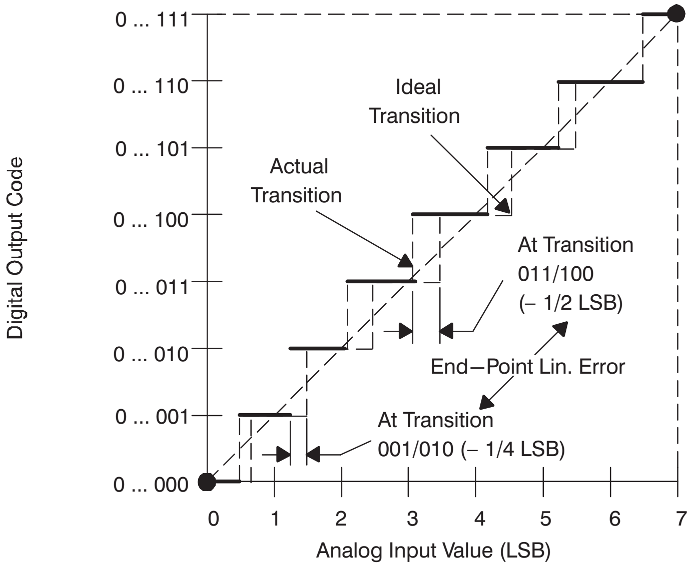
The differential nonlinearity error shown in Figure 19 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 19. Differential Nonlinearity (DNL)

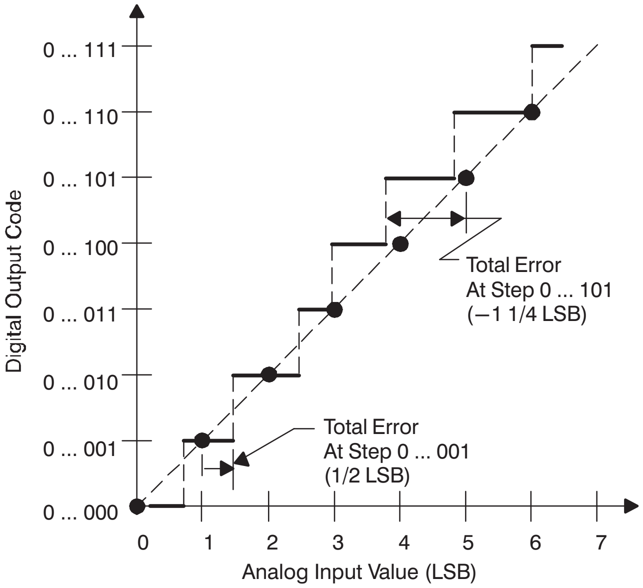
The integral nonlinearity error shown in Figure 20 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.



A. 1 LSB = (AD_{REFHI} - AD_{REFLO})/2^{10}

Figure 20. Integral Nonlinearity (INL) Error

The absolute accuracy or total error of an MibADC as shown in Figure 21 is the maximum value of the difference between an analog value and the ideal midstep value.



A. 1 LSB = (AD_{REFHI} - AD_{REFLO})/2^{10}

Figure 21. Absolute Accuracy (Total) Error

THERMAL CHARACTERISTICS

PARAMETER	°C/W
$R_{\theta JA}$	48
$R_{\theta JC}$	5

REVISION HISTORY

This revision history highlights the changes made to the device-specific datasheet SPNS099 to create the SPNS099A version.

Table 9. Revision History

SPNS099A to SPNS099B
Revised the Family Nomenclature drawing, Figure 2, to add Q version of the temperature range.
Revised "Absolute Maximum Ratings" table to add Q version of the temperature range.
Revised "Device Recommended Operating Conditions" table to add Q version of the temperature range.
Added note to $\overline{\text{PORRST}}$ Timing Diagram.
Changed T_A range to –40°C to 125°C on t_{wec} in "Timing Requirements for Program Flash" table.
Added t_{wec} MIN value of 50000 and deleted MAX value in "Timing Requirements for Program Flash" table.
Changed $t_{erase(sector)}$ TYP value to 1.7 and removed MAX value in "Timing Requirements for Program Flash" table.
SPNS099 to SPNS099A
In "Memory Selects" section, added decoded block size = 0x00100000.
Moved "XOR Share" section to "Description" section.
In "Flash Program and Erase" section, added information about executing from different banks and note about OTP sector.
Updated temperature range to T version, –40°C to 105°C, throughout.
Updated device identification code register value in "Device Identification Code Register."
Added "Device and Development-Support Tool Nomenclature" information.
Changed V_{CC} to 2.06 V from 2.05 V throughout.
Separate V_{IL} and V_{IH} values added for OSCIN in the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.
I_{CC} value at SYSCLK - 24 MHZ deleted in the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.
Removed "all frequencies" from halt test conditions, I_{CC}, in the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.
Operating I_{CC} value (pipeline mode) changed to 70 mA in the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.
I_{CCp} read operation value changed to 50 mA in the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.
$f_{(OSCRST)}$ value changed from MAX to TYP in "Timing Requirements for ZPLL Circuits Enabled or Disabled" table.
Moved 2.75 from Max to Min column for $V_{CCIOPORH}$ in "Timing Requirements for $\overline{\text{PORRST}}$" table.
Added row for T_{fsu} to "Switching Characteristics over Recommended Operating Conditions for $\overline{\text{RST}}$" table.
Updated $t_{prog(Total)}$ to 0.5 s typical and 2 s maximum.
Added rows for $T_{fp(RST)}$, $T_{fp(SLEEP)}$, and $T_{fp(STANDBY)}$ to "Flash Timings" table.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TMS470R1A64PNT	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168HR
TMX470R1A64PN	PREVIEW	LQFP	PN	80	1	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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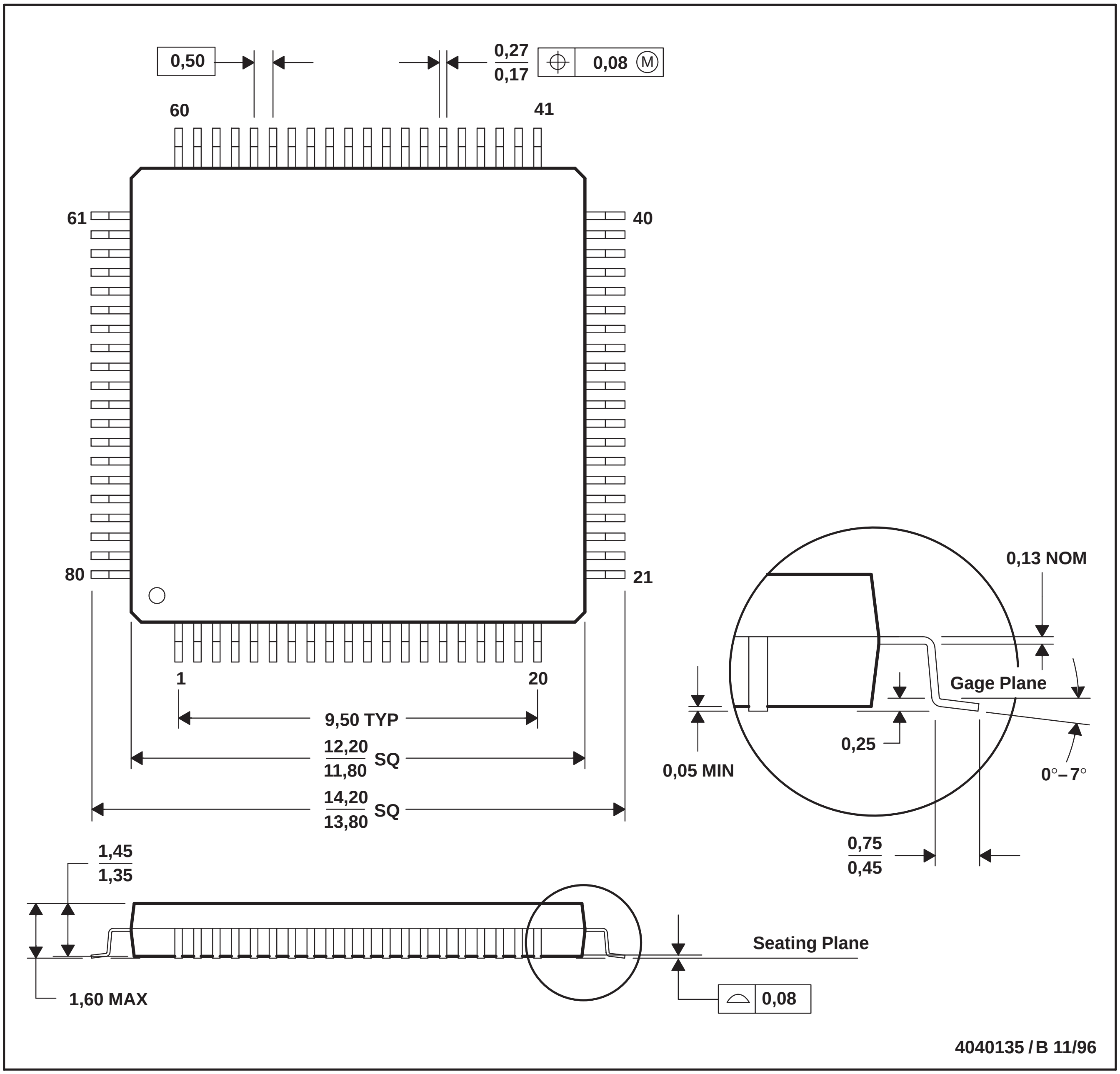
PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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Mailing Address: Texas Instruments
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