Digital Signal Controllers

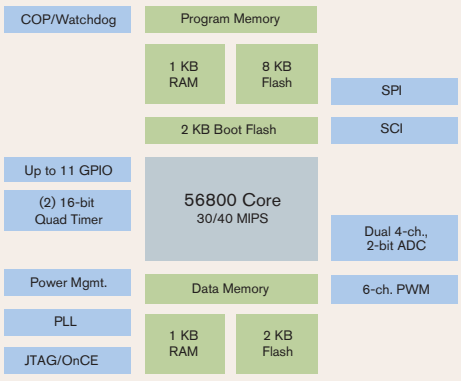
56F801

Target Applications

- > Pumps
- > Industrial fans
- > Exercise equipment
- > Smart appliances
- > Compressors
- > Noise cancellation
- > HVAC
- > Remote monitoring
- > Tachometers
- > Cable test equipment
- > General-purpose devices
- > Switched-mode power supplies

Overview

The 56F801 is a member of the 56800 core-based family of digital signal controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller (MCU) with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility and compact program code, the 56F801 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.



56800E Core Features	Benefits
> Efficient 16-bit 56800 family digital signal controller engine with dual Harvard architecture	> Onboard voltage regulator and power management is designed to reduce overall system cost by allowing for a single supply voltage
> As many as 40 MIPS at 80 MHz core frequency	> Internal relaxation oscillator for cost-sensitive applications by eliminating the need for an external crystal
> Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)	> Flash memory is engineered to provide reliable, nonvolatile memory storage, eliminating the need for external storage devices
> Two 36-bit accumulators, including extension bits	> Easy to program with flexible application development tools
> 16-bit bidirectional barrel shifter	> Simple updating of Flash memory through serial peripheral interface (SPI), serial communications interface (SCI) or OnCE port, using on-chip boot loader
> Parallel instruction set with unique addressing modes	> Program can boot directly from Flash
> Hardware DO and REP loops	> Supports multiple motors or multiphase control
> Three internal address buses	> Patented distortion correction in pulse-width modulation (PWM) for lower-risk, better performing control
> Four internal data buses	> PWM and analog-to-digital converter (ADC) modules are tightly coupled to reduce processing overhead
> Instruction set supports both DSP and controller functions	> Low-voltage interrupts (LVIs) protect the system during brownout or power failure
> Controller-style addressing modes and instructions for compact code	> Simple interface with other asynchronous serial communication devices and off-chip EE memory
> Efficient C compiler and local variable support	
> Software subroutine and interrupt stack with depth limited only by memory	
> JTAG/on-chip emulation (OnCE™) debug programming interface	

Energy Information

- > Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- > Uses a single 3.3V power supply
- > On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- > Wait and stop modes available

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56F801 16-bit Digital Signal Controller

> Up to 40 MIPS operation at 80 MHz core frequency

> DSP and MCU functionality in a unified, C-efficient architecture

> MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes

> 12 KB On-chip Flash

- 8 KB Program Flash
- 2 KB Data Flash
- 2 KB Boot Flash

> 1 KB Program RAM

> 1 KB Data RAM

> Hardware DO and REP loops

> 6-channel PWM module

> Two four-channel, 12-bit ADCs

> SCI

> SPI

> JTAG/OnCE port for debugging

> On-chip relaxation oscillator

> 48-pin LQFP package

> 11 shared general-purpose input/output (GPIO) pins

> Two general-purpose quad timers

56F801 Memory Features

> Harvard architecture permits as many as three simultaneous accesses to program and data memory

> On-chip memory including a low-cost, high-volume Flash solution

- 12 KB On-chip Flash
  - 8 KB Program Flash
  - 2 KB Data Flash
  - 2 KB Boot Flash
- 1 KB Program RAM
- 1 KB Data RAM

> Programmable Boot Flash supports customized boot code and field upgrades of stored code through a variety of interfaces (JTAG, CAN, SPI)

56F801 Peripheral Circuit Features

> PWM with six PWM outputs, two fault inputs and fault-tolerant design with dead-time insertion; supports both center- and edge-aligned modes

> Two 12-bit ADCs, which support two simultaneous conversions; ADC and PWM modules can be synchronized

> Two general-purpose quad timers

> SCI

> SPI

> 11 multiplexed GPIO pins

> Computer operating properly (COP)/ watchdog timer

> Two dedicated external interrupt pins

> External reset pin for hardware reset

> JTAG/OnCE for unobtrusive, processor speed-independent debugging

> Software-programmable, Phase-Lock Loop (PLL)-based frequency synthesizer

> Oscillator flexibility between either an external crystal oscillator or an on-chip relaxation oscillator

Award-Winning Development Environment

> Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.

> The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigating, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

Product Documentation

DSP56800 Family Manual	Detailed description of the 56800 family architecture and 16-bit DSP core processor and the instruction set ***Order Number:*** DSP56800FM
DSP56F80x User's Manual	Detailed description of memory, peripherals and interfaces of the 56F801, 56F802, 56F803, 56F805 and 56F807 ***Order Number:*** DSP56F801-7UM
DSP56F801 Technical Data Sheet	Electrical and timing specifications, pin descriptions and package descriptions ***Order Number:*** DSP56F801
DSP56F801 Product Brief	Summary description and block diagram of the core, memory, peripherals and interfaces ***Order Number:*** DSP56F801PB

Ordering Information

Part	DSP56F801
Supply Voltage	3.0V–3.6V
Package Type	Low-Profile Quad Flat Pack (LQFP)
Pin Count	48
Frequency (MHz)	80
Order Number	DSP56F801FA80

Part	DSP56F801
Supply Voltage	3.0V–3.6V
Package Type	Low-Profile Quad Flat Pack (LQFP)
Pin Count	48
Frequency (MHz)	60
Order Number	DSP56F801FA60

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