Overview

The 56F801 is a member of the 56800 core-based family of digital signal controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller (MCU) with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility and compact program code, the 56F801 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

Target Applications
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- Pumps
- Industrial fans
- Exercise equipment
- Smart appliances
- Compressors
- Noise cancellation
- HVAC

> Remote monitoring
> Tachometers
> Cable test equipment
> General-purpose devices
> Switched-mode power supplies

56800E Core Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefits</th>
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<tbody>
<tr>
<td>Efficient 16-bit 56800 family digital signal controller engine with dual Harvard architecture</td>
<td>Onboard voltage regulator and power management is designed to reduce overall system cost by allowing for a single supply voltage</td>
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<td>As many as 40 MIPS at 80 MHz core frequency</td>
<td>Internal relaxation oscillator for cost-sensitive applications by eliminating the need for an external crystal</td>
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<td>Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)</td>
<td>Flash memory is engineered to provide reliable, nonvolatile memory storage, eliminating the need for external storage devices</td>
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<td>Two 36-bit accumulators, including extension bits</td>
<td>Easy to program with flexible application development tools</td>
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<td>16-bit bidirectional barrel shifter</td>
<td>Simple updating of Flash memory through serial peripheral interface (SPI), serial communications interface (SCI) or OnCE port, using on-chip boot loader</td>
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<td>Parallel instruction set with unique addressing modes</td>
<td>Program can boot directly from Flash</td>
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<td>Hardware DO and REP loops</td>
<td>Supports multiple motors or multiphase control</td>
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<tr>
<td>Three internal address buses</td>
<td>Patented distortion correction in pulse-width modulation (PWM) for lower-risk, better performing control</td>
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<tr>
<td>Four internal data buses</td>
<td>PWM and analog-to-digital converter (ADC) modules are tightly coupled to reduce processing overhead</td>
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<td>Instruction set supports both DSP and controller functions</td>
<td>Low-voltage interrupts (LVIs) protect the system during brownout or power failure</td>
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<td>Controller-style addressing modes and instructions for compact code</td>
<td>Simple interface with other asynchronous serial communication devices and off-chip EE memory</td>
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<td>Efficient C compiler and local variable support</td>
<td>Energy Information</td>
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<td>Software subroutine and interrupt stack with depth limited only by memory</td>
<td>Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs</td>
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<td>JTAG/on-chip emulation (OnCE™) debug programming interface</td>
<td>Uses a single 3.3V power supply</td>
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Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and stop modes available

Digital Signal Controllers

56F801
**56F801 16-bit Digital Signal Controller**
- Up to 40 MIPS operation at 80 MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 12 KB On-chip Flash
  - 8 KB Program Flash
  - 2 KB Data Flash
  - 2 KB Boot Flash
- 1 KB Program RAM
- 1 KB Data RAM
- Programmable Boot Flash supports customized boot code and field upgrades of stored code through a variety of interfaces (JTAG, CAN, SPI)

**56F801 Peripheral Circuit Features**
- PWM with six PWM outputs, two fault inputs and fault-tolerant design with dead-time insertion; supports both center- and edge-aligned modes
- Two 12-bit ADCs, which support two simultaneous conversions; ADC and PWM modules can be synchronized
- Two general-purpose quad timers
- SCI
- SPI
- JTAG/OnCE port for debugging
- On-chip relaxation oscillator
- 6-channel PWM module
- Two four-channel, 12-bit ADCs
- SCI
- SPI
- JTAG/OnCE port for debugging
- On-chip relaxation oscillator
- 48-pin LQFP package
- 11 shared general-purpose input/output (GPIO) pins
- Two general-purpose quad timers

**56F801 Memory Features**
- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 12 KB On-chip Flash
  - 8 KB Program Flash

**Award-Winning Development Environment**
- Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.
- The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigating, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

**Learn More:** For more information about Freescale products, please visit [www.freescale.com](http://www.freescale.com).